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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Attorney Docket No.	1776/00039
First Named Inventor or Application Identifier	Fumitaka Sugaya
Title	A Semiconductor Device And A Method Of Manufacturing The Same
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: **Assistant Commissioner for Patents**
Box Applications
Washington, DC 20231

1. [X] Filing Fee as calculated below.
2. [X] Specification [Total Pages **51**]
   (preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Pages **33**]
4. Oath or Declaration [Total Pages **1**]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [X] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
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ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Other: Priority Claim from Jap 9-116322 filed April 18, 1997

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No. 09/059,590

18. CORRESPONDENCE ADDRESS

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INDEP	5	minus	3	= 2	x39=	$		x78=	$156
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	
Fumitaka SUGAYA	:	
Serial No. Unknown (Divisional of 09/059,590)	:	
Filed: September 1, 1999	:	
For: A SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME	:	Atty Docket: 1776/00039

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to fee calculation and examination on the merits, please amend the above-identified patent application as follows:

IN THE SPECIFICATION:

On page 1, enter: --This application is a divisional of Application Serial No. 09/059,590--.

IN THE CLAIMS:

Please cancel claims 1-27 and 46-47 elected in the parent case without prejudice to their reentry at some later date and examine non-elected claims 28-45 in this application.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

Title : A SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME

Inventor(s) : Fumitaka SUGAYA

ABSTRACT OF THE DISCLOSURE

A semiconductor device of the present invention is a semiconductor memory having a charge storage film. Recesses or holes which effectively increase the capacitance of a floating gate or a memory cell capacitor are formed in the charge storage film. These recesses or holes are formed at the same time the floating gate electrode or the lower electrode of the capacitor is isolated into the form of islands. A dielectric film and a polysilicon film is formed on the isolated island floating gate electrodes or lower electrodes. These recesses or holes increase the surface area of the dielectric film and improve the write and erase characteristics of a memory cell.

BACKGROUND OF THE INVENTION

[Field of the Invention]

The present invention relates to a semiconductor device including a memory cell having a composite gate structure or a semiconductor device including a stacked memory cell capacitor and a method of fabricating the same.

[Description of the Related Art]

Conventionally, several improvements have been made to improve the write and erase characteristics of a memory cell of an EEPROM or the like having a floating gate structure or a memory cell capacitor.

As an example, in prior art disclosed in Japanese Patent Laid-Open No. 5-110107, at least a portion of a polysilicon film as a floating gate electrode is formed by CVD under conditions by which a larger number of fine undulations are formed on the surface of the floating gate electrode, and an insulating interlayer and a control gate electrode are formed along the undulations on the surface of the floating gate electrode.

These fine undulations increase the capacitance between the floating gate electrode and a control gate electrode. When voltage drop in which the voltage applied to the control gate electrode decreases occurs, these undulations efficiently act on the floating gate electrode to improve the write and erase characteristics.

Also, in prior art disclosed in Japanese Patent Laid-Open No. 5-55605, a recess is formed in substantially the center of a floating gate electrode to increase the capacitance between the floating gate electrode and a control gate electrode. Consequently, an effect similar to

the effect of the above prior art is achieved.

The capacitance of a memory cell capacitor can also be increased by forming undulations on the surface of a lower electrode.

For example, Japanese Patent Laid-Open No. 5-243515 has described a method of increasing the charge storage amount by forming a rectangular or cylindrical trench in a lower electrode of a stacked memory cell capacitor.

Unfortunately, the above-mentioned prior arts have the following problems.

First, in the prior art disclosed in Japanese Patent Laid-Open No. 5-110107, the fine undulations on the floating gate electrode are formed under specific conditions by CVD. Therefore, the fabrication steps are complicated to set the CVD conditions. Additionally, since these undulations are very fine, the effect of increasing the capacitance is not satisfactory.

In the prior art disclosed in Japanese Patent Laid-Open No. 5-55605, the recess is formed in substantially the center of the floating gate electrode after a polysilicon film serving as the floating gate electrode is formed. Therefore, it is unavoidable to complicate the fabrication steps and increase the number of the fabrication steps. Also, the end point of etching for forming the recess is difficult to determine. Accordingly, the recess may sometimes extend through the polysilicon film to separate the floating gate electrode.

In the prior art of a capacitor disclosed in Japanese Patent Laid-Open No. 5-243515, the trench is formed by etching after stacked polysilicon serving as the lower

electrode is formed. Accordingly, the fabrication steps are complicated and the number of the fabrication steps is increased. Furthermore, the end point of the etching cannot be easily determined.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor device which includes a composite gate structure memory cell or a stacked memory cell capacitor, effectively increases the capacitance of the floating gate electrode or the memory cell capacitor, and has high reliability, and a simple method of fabricating this semiconductor device.

A semiconductor device of the present invention is a semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate, comprising an island-like charge storage film formed across the element isolation structure and the element active region so as to be formed on the element active region through an insulating film, the charge storage film having a recess in a surface on the element active region and a hole formed on the element isolation structure to reach the element isolation structure, a dielectric film so formed as to cover the surface of the charge storage film including inner surfaces of the hole, and a conductive film formed on the dielectric film and capacitively coupled with the charge storage film.

Another aspect of the semiconductor device of the present invention is a semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate, comprising

an island-like charge storage film formed across the element isolation structure and the element active region so as to be formed on the element active region through an insulating film, the charge storage film having a recess in a surface on the element active region and a hole formed on the element isolation structure to reach the element isolation structure, and a conductive film formed on the charge storage film.

Still another aspect of the semiconductor device of the present invention is a semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate and having a transistor constituted by a gate electrode and a pair of impurity diffusion layers in the element active region, comprising an insulating interlayer formed on the semiconductor substrate including the transistor, a first hole formed in the insulating interlayer and having a surface layer of the impurity diffusion layer as a bottom surface, an island-like charge storage film electrically connected to one of the impurity diffusion layers through the first hole, a second hole formed in the charge storage film and having a surface layer of the insulating interlayer as a bottom surface, a dielectric film so formed as to cover a surface of the charge storage film including inner surfaces of the second hole, and a conductive film formed on the dielectric film and capacitively coupled with the charge storage film, wherein the charge storage film, the dielectric film, and the conductive film constitute a capacitor.

Still another aspect of the semiconductor device of the

present invention is a semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate, comprising an insulating film formed on the semiconductor substrate in the element active region, and a charge storage film patterned on the insulating film, wherein the charge storage film is formed across the element isolation structure and has a hole on the element isolation structure, and at least a portion of a bottom surface of the hole reaches a surface layer of the element isolation structure.

Still another aspect of the semiconductor device of the present invention is a semiconductor device including a plurality of element isolation regions defined by forming an element isolation structure on a semiconductor substrate, comprising an island-like charge storage film formed across the element isolation structure and the element active regions and having a recess, a dielectric film so formed as to cover a surface of the charge storage film, and a conductive film formed on the dielectric film and capacitively coupled with the charge storage film, wherein the charge storage film is formed in each of the element active regions, and an upper surface of each of the charge storage films is planarized by CMP and flush with an upper surface of an adjacent charge storage film.

A method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming an insulating film on the semiconductor substrate in the element active region, the

third step of forming a first conductive film on an entire surface of the semiconductor substrate including the insulating film and the element isolation structure, the fourth step of forming a mask pattern having first and second openings on the first conductive film, the fifth step of etching the first conductive film until the element isolation structure is exposed in the first opening by using the mask pattern as a mask, thereby dividing the first conductive film, and simultaneously forming a recess in the second opening by leaving the first conductive film behind on a bottom, the sixth step of forming a dielectric film so as to cover a surface of the first conductive film, and the seventh step of forming a second conductive film on the dielectric film and opposing the second conductive film to the first conductive film through the dielectric film.

Another aspect of the method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming a gate insulating film and a gate electrode in the element active region, the third step of doping an impurity into the second substrate to form a pair of impurity diffusion layers in surface regions of the semiconductor substrate on two sides of the gate electrode, the fourth step of forming a first conductive film electrically connected to one of the impurity diffusion layers, the fifth step of forming a mask pattern having at least first and second openings on the first conductive film, the sixth step of etching the first conductive film by using the mask pattern as a mask,

thereby dividing the first conductive film in the first opening, and simultaneously forming a recess in the second opening by leaving the first conductive film behind on a bottom, the seventh step of forming a dielectric film so as to cover a surface of the first conductive film, and the eighth step of forming a second conductive film on the dielectric film and opposing the second conductive film to the first conductive film through the dielectric film.

Still another aspect of the method of fabricating a semiconductor device according to the present invention comprises the first step of forming a first conductive film in an insulating film region on a semiconductor substrate, the second step of forming a mask pattern having two types of openings on the first conductive film, the third step of etching the first conductive film by using the mask pattern as a mask, thereby dividing the first conductive film conforming to a shape of one of the openings, and simultaneously forming at least one recess in a surface of the divided first conductive film conforming to a shape of the other opening, the fourth step of forming an insulating film so as to cover a surface of the first conductive film, and the fifth step of forming a second conductive film so as to cover a surface of the insulating film and opposing the second conductive film to the first conductive film through the insulating film.

Still another aspect of the method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming an

insulating film on the semiconductor substrate in the element active region, the third step of forming a first conductive film on an entire surface including the insulating film and the element isolation structure, the fourth step of forming a mask pattern having at least first and second openings on the first conductive film, the fifth step of etching the first conductive film until the element isolation structure is exposed in the first and second openings by using the mask pattern as a mask, thereby dividing the first conductive film below the first opening, and simultaneously forming a hole extending through the first conductive film below the second opening, the sixth step of forming a dielectric film so as to cover the first conductive film, and the seventh step of forming a second conductive film on the dielectric film and opposing the second conductive film to the first conductive film through the dielectric film.

Still another aspect of the method of fabricating a semiconductor device according to the present invention comprises the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate, the second step of forming a gate oxide film and a gate electrode on the semiconductor substrate in the element active region, the third step of doping an impurity into the semiconductor substrate in the element active region to form a pair of impurity diffusion layers in surface regions of the semiconductor substrate on two sides of the gate electrode, the fourth step of forming a first conductive film electrically connected to one of the impurity diffusion layers, the fifth step of forming a mask

pattern having at least first and second openings on the first conductive film, the sixth step of etching the first conductive film by using the mask pattern as a mask, thereby dividing the first conductive film below the first opening, and simultaneously forming a hole extending through the first conductive film below the second opening, the seventh step of forming a dielectric film so as to cover a surface of the first conductive film, and the eighth step of forming a second conductive film so as to cover the dielectric film and opposing the second conductive film to the first conductive film through the dielectric film.

In the semiconductor device of the present invention, a recess or a hole is formed in the charge storage film. Therefore, the area of the dielectric film can be increased to increase the charge storage amount. Especially when a hole is formed, the charge storage film and the conductive film can be opposed to each other through the dielectric film within the range from the lower surface to the upper surface of the hole. Consequently, the charge storage amount can be effectively increased.

In the method of fabricating a semiconductor device of the present invention, the first conductive film (charge storage film) is divided by etching along the first opening in a mask pattern. At the same time, a recess or hole can be formed by self-alignment along the second opening in the mask pattern.

By setting the width of the first opening to be twice or more the width of the second opening, it is possible to decrease the etching rate in the second opening by a microloading effect and reliably form the recess without

dividing the first conductive film.

Also, when the first conductive film is formed across the step between the element isolation structure and the element active region, the first conductive film is etched after its surface is planarized by polishing. Accordingly, even when etching is performed until the element isolation structure is exposed along the first opening, a recess can be formed without dividing the first conductive film in the second opening formed above the element active region.

When a hole is to be formed in the first conductive film, the first conductive film is etched until the underlying stacked film is exposed in the first and second openings. Consequently, it is possible to divide the first conductive film along the first opening and form a hole along the second opening.

The present invention can provide a semiconductor device which includes a composite gate structure memory cell or a stacked memory cell capacitor and in which the capacitance of the floating gate or the memory cell capacitor is effectively increased, and a method of stably and reliably fabricating this semiconductor device.

Accordingly, the present invention contributes to further development of these semiconductor devices.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1G are schematic sectional views showing a method of fabricating an EEPROM according to the first embodiment in order of steps;

Figs. 2A to 2J are schematic sectional views showing the method of fabricating the EEPROM according to the first embodiment in order of steps;

Fig. 3 is a schematic plan view showing the EEPROM according to the first embodiment;

Figs. 4A to 4C are schematic sectional views showing a method of fabricating an EEPROM according to a modification of the first embodiment in order of steps;

Fig. 5 is a schematic plan view showing the EEPROM according to the modification of the first embodiment shown in Figs. 4A to 4C;

Figs. 6A to 6C are schematic views showing a method of fabricating an EEPROM according to another modification of the first embodiment in order of steps;

Fig. 7 is a schematic view showing the EEPROM according to the modification of the first embodiment shown in Figs. 6A to 6C;

Figs. 8A to 8D are schematic sectional views showing a method of fabricating an EEPROM according to the second embodiment in order of steps;

Fig. 9 is a schematic plan view showing the EEPROM according to the second embodiment;

Figs. 10A to 10K are schematic sectional views showing a method of fabricating a stacked capacitor cell structure DRAM according to the third embodiment in order of steps;

Fig. 11 is a schematic plan view showing the stacked capacitor cell structure DRAM according to the third embodiment;

Figs. 12A to 12E are schematic sectional views showing a method of fabricating a stacked capacitor cell structure DRAM according to a modification of the third embodiment in order of steps;

Fig. 13 is a schematic plan view showing the stacked

capacitor cell structure DRAM according to the modification of the third embodiment shown in Figs. 12A to 12E;

Figs. 14A to 14E are schematic sectional views showing a method of fabricating a stacked capacitor cell structure DRAM according to another modification of the third embodiment in order of steps;

Fig. 15 is a schematic plan view showing the stacked capacitor cell structure DRAM according to the modification of the third embodiment shown in Figs. 14A to 14E;

Fig. 16 is a schematic plan view showing the EEPROM according to the first embodiment; and

Fig. 17 is a flow chart showing a read method of the EEPROM according to the first embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

-First Embodiment-

The arrangement of a memory cell of an EEPROM according to the first embodiment of the present invention and a method of fabricating the same will be described below. Figs. 1A to 1G and 2A to 2J are side sectional views showing the fabrication steps of the EEPROM memory cell according to the first embodiment. Fig. 3 is a schematic plan view showing a memory cell region of the EEPROM. A section Ⅰ-Ⅰ in Fig. 3 corresponds to Figs. 1A to 1G; and a section Ⅱ-Ⅱ, to Figs. 2A to 2J.

First, the surface of a p-type silicon semiconductor substrate 1 is selectively oxidized by a so-called LOCOS process to form a field oxide film 2. Consequently, element isolation is achieved on the p-type silicon semiconductor substrate 1 to define element formation regions 3.

Subsequently, the element formation regions on the p-type silicon semiconductor substrate 1 are thermally oxidized to form a tunnel oxide film 4 having a thickness of about 100 Å , thereby obtaining the state shown in Figs. 1A and 2A. Thereafter, a polysilicon film 5 having a thickness of about 5,000 Å is formed on the entire surface of the field oxide film 2 and the tunnel oxide film 4 by adding a dopant gas by low-pressure CVD. Alternatively, an undoped polysilicon film 5 may be formed and given conductivity by ion-implanting an impurity such as arsenic. This state is shown in Fig. 2B.

Next, a photoresist 6 is formed on the polysilicon film 5 by photolithography. In this photolithography, as shown in Fig. 1B, a photoresist opening 7 is formed by forming an opening about 0.6 μ m wide in a region for isolating floating gate electrodes 9 to be formed later. Also, photoresist openings 8 are formed by forming openings about 0.25 μ m wide in regions corresponding to substantially the center of the width of the tunnel oxide film 4.

By using the photoresist 6 as a mask, the polysilicon film 5 is selectively removed by dry etching until the surface of the field oxide film 2 below the photoresist opening 7 is exposed. Since the width of the photoresist openings 8 is smaller than the half width of the photoresist opening 7, the supply of the etchant is reduced by a microloading effect when the polysilicon film 5 exposed in the photoresist openings 8 is etched. As a consequence, the etching rate is decreased in these portions.

That is, the progress in etching the polysilicon film 5 exposed in the photoresist opening 7 is faster than the

progress in etching the polysilicon film 5 exposed in the photoresist openings 8. Accordingly, the polysilicon film 5 exposed in the photoresist opening 7 is removed first, and the underlying field oxide film 2 is exposed.

The dry etching is stopped when the field oxide film 2 is exposed in the photoresist opening 7. Consequently, the polysilicon film 5 is separated in the position of the photoresist opening 7, forming the floating gate electrodes 9. In the positions of the photoresist openings 8, the polysilicon film 5 remains on the bottom surfaces to form recesses 20 on the floating gate electrodes 9. This state is shown in Figs. 1C and 2C.

Subsequently, as shown in Figs. 1D and 2D, a silicon oxide film about 50 Å thick, a silicon nitride film about 40 Å thick, and a silicon oxide film about 50 Å thick are deposited in this order on the entire surface by LPCVD, thereby forming a dielectric film 10 made from an ONO film.

As shown in Figs. 1E and 2E, a polysilicon film 11 having a thickness of about 1,500 Å is formed on the dielectric film 10 by CVD and patterned together with the floating gate electrodes 9 and the dielectric film 10, thereby completing composite gate electrodes 12. This state is shown in Figs. 1E and 2F. The floating gate electrodes 9 have the function of a charge storage film which stores electric charge in accordance with the voltage applied to the polysilicon film 11.

By using the composite gate electrodes 12 as masks, arsenic is ion-implanted into the surface region of the p-type silicon semiconductor substrate 1 to form a source region 13 and a drain region 14 as n-type impurity

diffusion layers. Appropriate ion-implantation conditions are an acceleration energy of about 70 keV and a dose of about 5 x $10^{15}/cm^2$. Thereafter, annealing is performed at 900℃ for about 30 min to activate the implanted arsenic, obtaining the state shown in Fig. 2G.

Next, as shown in Fig. 2H, a BPSG film 15 as an insulating interlayer is deposited on the entire surface by CVD, and the surface is planarized by reflow. Thereafter, contact holes 16, 17, and 18 are formed in the BPSG film 15 to expose portions of the source region 13, the polysilicon film 11, and the drain region 14, respectively. The result is the state shown in Fig. 2I.

After an aluminum alloy film 19 is deposited by sputtering to bury the contact holes 16, 17, and 18, a wiring pattern is formed by photolithography and subsequent dry etching to complete a memory cell of an EEPROM as shown in Figs. 1F, 2J, and 3.

Note that the element formation regions 3 defined in the first step can also be defined by a method other than LOCOS. When the regions are to be defined by a so-called field shield structure, a shield gate oxide film is first formed on the p-type semiconductor substrate 1, and a thin polysilicon film and a CVD oxide film are formed in this order on top of the shield gate oxide film.

Subsequently, patterning is performed to remove the above stacked structure except for portions serving as the element isolation regions. Thereafter, a CVD oxide film is formed, and anisotropic etching is performed to leave this CVD oxide film only on the side walls of the patterned stacked structure described above, thereby forming the

element isolation regions. Fig. 1G shows a memory cell of an EEPROM having a field shield element isolation structure thus formed. In Fig. 1G, a thin polysilicon film 24 covered with a CVD oxide film 23 is equivalent to a shield plate electrode.

It is also possible to define element active regions by a trench element isolation structure formed by burying an insulating film in a trench formed in a semiconductor substrate.

In the first embodiment as described above, in separating the adjacent floating gate electrodes 9 of a memory cell of an EEPROM, the width of the photoresist openings 8 is made smaller than the half width of the photoresist opening 7. Consequently, even when the polysilicon film 5 exposed in the photoresist opening 7 is etched away to expose the underlying field oxide film 2, the polysilicon film 5 is left behind on the bottom surfaces of the photoresist openings 8 by the microloading effect, forming the recesses 20 in these portions.

Since etching is stopped when the field oxide film 2 is exposed, the bottom surfaces of the recesses 20 are reliably positioned above the surface of the field oxide film 2 by the microloading effect. This prevents the polysilicon film 5 from being divided by the recesses 20. Accordingly, the floating gate electrodes 9 having the recesses 20 can be stably formed.

Also, the recesses 20 are formed by self-alignment at the same time the floating gate electrodes 9 are separated. Therefore, the recesses 20 can be formed without increasing the number of fabrication steps.

In the composite gate electrode 12 including the floating gate electrode 9 having the recess 20, the dielectric film 10 made from an ONO film, and the polysilicon film 11, the capacitance of the dielectric film 10 is increased by the recess 20. As a consequence, the write and erase characteristics of the memory cell can be improved.

-Modifications-

A modification of the first embodiment will be described below. Figs. 4A to 4C are side sectional views showing the steps in fabricating a memory cell of an EEPROM according to this modification. Fig. 5 is a schematic plan view showing a memory cell region of this EEPROM. A section I - I in Fig. 5 corresponds to Figs. 4A to 4C. The same reference numerals as in the EEPROM of the first embodiment denote the same parts, and a detailed description thereof will be omitted.

Fig. 4A corresponds to the step shown in Fig. 1B of the first embodiment. In this modification, the steps up to the state shown in Fig. 4A are the same as in the first embodiment. As shown in Fig. 4A, the number of openings in the photoresist 6 formed on the polysilicon film 5 is larger than in the first embodiment.

That is, as shown in Fig. 4A, substantially cylindrical photoresist openings 21 are formed between the photoresist openings 7 and the photoresist opening 8 in this modification.

By using this photoresist 6 as a mask, the polysilicon film 5 is selectively removed by dry etching. The etching is performed until the underlying field oxide film 2 is

exposed in the photoresist opening 8 and the photoresist openings 21. Consequently, as shown in Fig. 4B, substantially cylindrical openings 22 are formed, and the recesses 20 are formed in the photoresist openings 7.

Thereafter, as in the first embodiment, the dielectric film 10 made from an ONO film is formed on the entire surface. The polysilicon film 11 is then formed by CVD and patterned to form the composite gate electrodes 12.

As in the first embodiment, arsenic is ion-implanted to form the source and drain regions 13 and 14 (not shown), the BPSG film 15 is deposited and subjected to reflow, the contact holes 16, 17, and 18 are formed, and the aluminum alloy film 19 is deposited and patterned to complete a memory cell of an EEPROM as shown in Figs. 4C and 5.

In the memory cell of the EEPROM according to the modification with the above arrangement, the substantially cylindrical openings 22 are additionally formed on the floating gate electrodes 9. Accordingly, the capacitance of the dielectric film 10 can be further increased compared to the first embodiment. As a consequence, the write and erase characteristics of the memory cell can be further improved.

Note that the etching rate controlled by the microloading effect can be increased or decreased by properly changing the diameter of the photoresist openings 21 in the above modification. For example, the diameter may be made smaller than in the above modification to set the same etching rate as the photoresist openings 7, and the polysilicon film 5 may be removed to the extent to which the underlying field oxide film 2 is not exposed.

If this is the case, in the step shown in Fig. 4A, substantially cylindrical photoresist openings 26 having a smaller diameter are formed between the photoresist openings 7 and 8 as shown in Fig. 6A.

By using this photoresist 6 as a mask, the polysilicon film 5 is selectively removed by dry etching. In this etching, the polysilicon film 5 exposed in the photoresist openings 26 is also removed to form substantially cylindrical recesses 25 as shown in Fig. 6B.

After the dielectric film 10 made from an ONO film is formed on the entire surface, the polysilicon film 11 is formed by CVD and patterned to form the composite gate electrodes 12.

Thereafter, arsenic is ion-implanted to form the source and drain regions 13 and 14, the BPSG film 15 is deposited on the entire surface and subjected to reflow, the contact holes 16, 17, and 18 are formed, and the aluminum alloy film 19 is deposited and patterned to complete a memory cell of an EEPROM as shown in Fig. 6C and the schematic plan view of Fig. 7.

As described above, even when the recesses 25 are formed by giving the microloading effect to the photoresist openings 26 by decreasing the diameter of the photoresist openings 26, the capacitance of the dielectric film 10 can be increased compared to the first embodiment. Consequently, the write and erase characteristics of the memory cell can be improved.

-Second Embodiment-

The arrangement of an EEPROM according to the second embodiment of the present invention and a method of

fabricating the same will be described below. Figs. 8A to 8D are side sectional views showing the steps in fabricating a memory cell of the EEPROM according to the second embodiment. Fig. 9 is a schematic plan view showing a memory cell region of this EEPROM. A section I - I in Fig. 9 corresponds to Figs. 8A to 8D. The same reference numerals as in the EEPROM of the first embodiment denote the same parts, and a detailed description thereof will be omitted.

This second embodiment differs from the first embodiment in that after a polysilicon film 5 is formed, the surface of the polysilicon film 5 is planarized by chemical mechanical polishing (CMP) before the step of forming a photoresist 6.

Fig. 8A is a view corresponding to the step shown in Fig. 2B of the first embodiment. Referring to Fig. 8A, the polysilicon film 5 having a thickness of about 1,000 Å is formed by LPCVD on a field oxide film 2 and a gate oxide film 4. The steps up to the state shown in Fig. 8A are the same as in the first embodiment.

Thereafter, as shown in Fig. 8B, the surface of the polysilicon film 5 is planarized by chemical mechanical polishing (CMP).

As shown in Fig. 8C, the photoresist 6 is formed on the polysilicon film 5. In the formation of this photoresist 6, a photoresist opening 7 is formed by forming an opening about 0.6 μm wide in a region for isolating floating gate electrodes 9 to be formed later. Also, photoresist openings 8 are formed by forming openings about 0.6 μm wide in portions above regions corresponding to the centers of

the floating gate electrodes 9.

The polysilicon film 5 is dry-etched by using the photoresist 6 as a mask, and the etching is stopped when the field oxide film 2 is exposed in the photoresist opening 7. The surface of the polysilicon film 5 is previously planarized by chemical mechanical polishing described above. Therefore, when etching is stopped at the time the field oxide film 2 is exposed, the tunnel oxide film 4 is not exposed and recesses 20 are formed in the photoresist openings 8 due to the step between the surfaces of the field oxide film 2 and the tunnel oxide film 4.

Accordingly, the recesses 20 can be formed with high controllability at the same time the floating gate electrodes 9 are isolated. This state is shown in Figs. 8D and 9.

Thereafter, as in the first embodiment, a dielectric film 10 made from an ONO film (not shown) is formed, a polysilicon film 11 is formed by CVD, and these films are patterned to form composite gate electrodes 12.

Following the same procedure as in the first embodiment, arsenic is ion-implanted into the p-type semiconductor substrate, a BPSG film 15 (not shown) is formed, and reflow is performed. Finally, contact holes 16, 17, and 18 are formed, and an aluminum alloy film 19 is formed and patterned to complete a memory cell of an EEPROM.

In the second embodiment as described above, the surface of the polysilicon film 5 is planarized before the photoresist 6 is formed. Therefore, even when etching is performed until the field oxide film 2 is exposed in the

photoresist opening 7, the recesses 20 can be reliably formed in the photoresist openings 8 without exposing the underlying tunnel oxide film 4.

By sufficiently increasing the height of the step between the surface of the tunnel oxide film 4 and the surface of the field oxide film 2, the recesses 20 can be formed by leaving the polysilicon film 5 behind on the bottom surfaces with higher controllability.

Also, in the second embodiment, the recesses 20 can also be formed by self-alignment when the floating gate electrodes 9 are isolated.

Furthermore, the photoresist 6 is formed on the planarized polysilicon film 5 and patterned by lithography. Therefore, the widths of the photoresist openings 7 and 8 can be set with high controllability during lithography.

In the above first and second embodiments, a nonvolatile memory such as an EEPROM or an EPROM using the floating gate electrodes 9 made from polysilicon as a charge storage film is described. However, a stacked film of a silicon oxide film, a silicon nitride film, and a silicon oxide film may be used as a charge storage film, and the present invention may be applied to an MONOS type nonvolatile memory including this charge storage film, a control gate, a source, and a drain. The present invention may also be applied to an MNOS type nonvolatile memory including a charge storage film made from a stacked film of a silicon oxide film and a silicon nitride film, a control gate, a source, and a drain. When a charge storage film is made from an insulating film as described above, the dielectric film 10 need not be formed. If this is the case,

electric charge is stored in the interface of the silicon oxide film or the silicon nitride film.

Fig. 16 is a schematic plan view showing an embodiment in which the source region 13 is formed by a diffusion layer commonly to the unit memory cells, and the gate electrode 22 of the access transister is formed commonly to the unit memory cells, over the first and second embodiments above described.

Furthermore, if storage information is binary data, the EEPROM can also be constituted as a so-called multi-valued memory by setting a predetermined value of two bits or more as a storage state. That is, if the storage state is n bits (2n values, n is an integer of 2 or more), it is only necessary to set 2n different threshold voltages. For example, if the storage state is two bits (four values), four different reference voltages (threshold voltages) are used in a one-to-one correspondence with storage states "00", "01", "10", and "11". In a read, one storage state of each memory cell of the EEPROM is specified from the four threshold voltages by a predetermined determining operation. If the storage state is three bits (eight values), eight different reference voltages (threshold voltages) are used in a one-to-one correspondence with storage states "000", "001", "010", "011", "100", "101", "110", and "111". In a read, one storage state of each memory cell of the EEPROM is specified from the eight threshold voltages by a predetermined determining operation. In addition to the various effects described earlier, this multi- valued EEPROM greatly increases the storage density of each memory cell. Therefore, the EEPROM

can well meet demands for a higher integration degree and a finer structure. If storage information is not binary data but information constituted by 0, 1, and 2, it is also possible to use "0", "1", and "2", or "00", "01", "02", "10", "11", "12", "20", "21", and "22" as storage states. The storage state is expressed by three values in the former case and nine values in the latter case. This multi-valued structure is also applicable to a DRAM (to be described later) and other various semiconductor memories as well as to the EEPROM.

A method of writing storage information when the EEPROM described above is a multi-valued memory capable of storing 2-bit nformation in each memory cell will be described below. First, to write storage information "11", the drain region 14 of a memory cell is connected to the ground potential, the source region 13 is opened, and a voltage of about 22 V is applied to the polysilicon film 11. Consequently, electrons are injected from the drain region 14 into the floating gate electrode 9 through the tunnel oxide film 4, and the threshold voltage (V_T) goes positive. Accordingly, the threshold voltage of the memory cell rises to about 4 V. This storage state is "11".

To write data "10", the drain region 14 of the memory cell is connected to the ground potential, the source region 13 is opened, and a voltage of about 20 V is applied to the polysilicon film 11. Consequently, electrons are injected from the drain region 14 into the floating gate electrode 9 through the tunnel oxide film 4, and the threshold voltage of the memory cell changes to about 3 V. This storage state is "10".

To write data "01", the drain region 14 of the memory cell is connected to the ground potential, the source region 13 is opened, and a voltage of about 18 V is applied to the polysilicon film 11. Consequently, electrons are injected from the drain region 14 into the floating gate electrode 9 through the tunnel oxide film 4, and the threshold voltage of the memory cell changes to about 2 V. This storage state is "01".

To write data "00", the drain region 14 of the memory cell is connected to the ground potential, the source region 13 is opened, and a voltage of about 10 V is applied to the polysilicon film 11. Consequently, the electrons injected into the floating gate electrode 9 are cleared from the drain region 14, and the threshold voltage of the memory cell changes to about 1 V. This storage state is "00".

Individual steps of a read method when the EEPROM described above is a multi-valued memory capable of storing 2-bit information in each memory cell will be described below with reference to Fig. 17. First, whether the upper bit of storage information stored in a memory cell is "0" or "1" is checked. To this end, a voltage of about 5 V is applied to the source region 13 and the drain region 14 and the polysilicon film 11 (step S1). The drain current is detected by a sense amplifier, and the threshold voltage V_T is compared with the threshold voltage of a comparative transistor Tr1 (step S2). If the threshold voltage V_T is larger than the threshold voltage of the transistor Tr1, it is determined that the upper bit is "1". If the current of the transistor Tr1 is smaller, it is determined that the

upper bit is "0".

If the threshold voltage V_T is larger than the threshold voltage of the transistor Tr1, a similar read is performed by using a transistor Tr2, and the current flowing through the memory cell is compared with the current flowing through the transistor Tr2 (step S3). If the threshold voltage V_T is smaller than the threshold voltage of the transistor Tr1, a similar read is performed by using a transistor Tr3 (step S4).

If the threshold voltage V_T is larger than the threshold voltage of the transistor Tr2 in the read performed in step S3, it is determined that the storage information stored in the memory cell is "11" (step S5), and the information is read out from the memory cell. On the other hand, if the threshold voltage V_T is smaller than the threshold voltage of the transistor Tr2 in step S3, it is determined that the storage information stored in the memory cell is "10" (step S6), and the information is read out from the memory cell.

If the threshold voltage of the memory cell is larger than the threshold voltage of the transistor Tr3 in step S4, it is determined that the storage information stored in the memory cell is "01" (step S7), and the information is read out from the memory cell. If the threshold voltage V_T is smaller than the threshold voltage of the transistor Tr3 in step S4, it is determined that the storage information stored in the memory cell is "00" (step S8), and the information is read out from the memory cell.

-Third Embodiment-

The arrangement of a stacked capacitor cell structure

DRAM according to the third embodiment of the present invention and a method of fabricating the same will be described below. Figs. 10A to 10K are side sectional views showing the steps in fabricating two adjacent DRAM memory cells in the third embodiment. Fig. 11 is a schematic plan view showing these DRAM memory cell regions. A section I - I in Fig. 11 corresponds to Figs. 10A to 10K.

First, as shown in Fig. 10A, the surface of a p-type silicon semiconductor substrate 31 is selectively oxidized by a so-called LOCOS process to form a field oxide film 32. Consequently, element isolation is achieved on the p-type silicon semiconductor substrate 31 to define two element formation regions 32.

Subsequently, the surface of the element formation regions 32 is thermally oxidized to form a gate oxide film 34 having a thickness of about 130 Å. Thereafter, a polysilicon film 35 is formed on the entire surface by CVD.

The gate oxide film 34 and the polysilicon film 35 are then patterned by photolithography and subsequent dry etching, thereby forming gate electrodes 36. This state is shown in Fig. 10B.

By using the gate electrodes 36 as masks, arsenic is ion-implanted to form source regions 37 and drain regions 38 as n-type impurity diffusion layers. Annealing is then performed to activate the arsenic ions. Appropriate ion-implantation conditions are an acceleration energy of about 70 keV and a dose of about $5 \times 10^{15}/cm^2$. Appropriate annealing conditions are a temperature of 900℃ and an annealing time of about 30 min. Consequently, n-type MOS transistors are formed on the p-type silicon substrate 31 as

shown in Fig. 10C.

Next, as shown in Fig. 10D, a BPSG film 39 as an insulating interlayer is formed on the entire surface of the p-type silicon semiconductor substrate 31 by CVD, and the surface is planarized by reflow.

As shown in Fig. 10E, holes 40 for exposing portions of the source regions 27 are formed in the BPSG film 39. Thereafter, a polysilicon film 41 is formed in the holes 40 and on the BPSG film 39 by adding a dopant gas by low-pressure CVD. Alternatively, an undoped polysilicon film 41 may be formed on the BPSG film 39 and given conductivity by ion-implanting an impurity such as arsenic. This state is shown in Fig. 10F.

Subsequently, a photoresist 42 is formed on the polysilicon film 41 by photolithography. In this photolithography, as shown in Fig. 10G, a photoresist opening 43 is formed by forming an opening about 0.6 μm wide in a region for isolating lower electrodes 48 of adjacent stacked capacitor cells to be formed later. Also, photoresist openings 44 are formed by forming openings about 0.25 μm wide in regions near the centers of the lower electrodes 48 to be formed.

By using the photoresist 42 as a mask, the polysilicon film 41 is selectively removed by dry etching. Since the width of the photoresist openings 44 is smaller than the half width of the photoresist opening 43, the supply of the etchant is reduced by a microloading effect when the polysilicon film 41 exposed in the photoresist openings 44 is etched. As a consequence, the etching rate is decreased in these portions.

That is, the progress in etching polysilicon film 41 exposed in the photoresist opening 43 is faster than the progress in etching the polysilicon film 41 exposed in the photoresist openings 44. Accordingly, the polysilicon film 41 exposed in the photoresist opening 43 is removed first, and the underlying BPSG film 39 is exposed.

This dry etching is stopped when the BPSG film 39 is exposed in the photoresist opening 43. Consequently, the polysilicon film 41 is separated in the position of the photoresist opening 43, forming the lower electrodes 48 of the stacked capacitor cells. In the positions of the photoresist openings 44, the polysilicon film 41 remains on the bottom surfaces to form recesses 49 in the lower electrodes 48. This state is shown in Fig. 10H.

Next, a silicon nitride film about 30 Å thick is deposited on the entire surface by LPCVD and oxidized in an oxygen atmosphere at about 850℃, thereby forming a dielectric film 45 made from an ONO film.

A polysilicon film 46 having a thickness of about 1,500 Å and serving as an upper electrode of the stacked capacitor cells is formed on the dielectric film 45 by CVD and patterned together with the dielectric film 45, thereby completing a stacked capacitor cell structure including the lower electrodes 48, the dielectric film 45, and the polysilicon film 46 as an upper electrode as shown in Fig. 10I. In this structure, the lower electrodes 48 achieve the function of charge storage films which capacitively couple with the polysilicon film 46 through the dielectric film 45.

Subsequently, as shown in Fig. 10J, a BPSG film 50 is

formed on the entire surface and subjected to reflow, and contact holes 47 are formed to expose portions of the drain regions 38. Thereafter, an aluminum alloy film 51 as a bit line is filled in the contact holes 47 and deposited on the BPSG film by sputtering. Finally, the aluminum alloy film 51 is patterned to complete a stacked capacitor cell structure DRAM as shown in Figs. 10K and 11.

In the third embodiment as described above, in separating the adjacent lower electrodes 48 in the stacked capacitor cell structure DRAM, the width of the photoresist openings 44 is made smaller than the half width of the photoresist opening 43. Consequently, even when the polysilicon film 41 exposed in the photoresist opening 43 is etched away until the underlying BPSG film 39 is exposed, the polysilicon film 41 is left behind on the bottom surfaces of the photoresist openings 44 by the microloading effect, forming the recesses 49 in these portions.

Since etching is stopped when the BPSG film 39 is exposed, the bottom surfaces of the recesses 49 are reliably positioned above the surface of the BPSG film 39 by the microloading effect. This prevents the polysilicon film 41 from being separated by the recesses 20. Accordingly, the lower electrodes 48 having the recesses 49 can be stably formed.

Also, the recesses 49 are formed by self-alignment at the same time the lower electrodes 48 are isolated. Therefore, the recesses 49 can be formed without increasing the number of fabrication steps.

In each stacked capacitor cell including the lower

electrode 48 having the recess 49, the dielectric film 45 made from the ONO film, and the polysilicon film 46 as the upper electrode, the capacitance of the dielectric film 45 is increased by the recess 49. As a consequence, the write and erase characteristics of the memory cell can be improved.

-Modifications-

A modification of the third embodiment will be described below. Figs. 12A to 12E are side sectional views showing the steps in fabricating two adjacent DRAM memory cell capacitors according to this modification. Fig. 13 is a schematic plan view showing the memory cell capacitors. A section I -I in Fig. 13 corresponds to Figs. 12A to 12E. The same reference numerals as in the DRAM of the third embodiment denote the same parts, and a detailed description thereof will be omitted.

Fig. 12A corresponds to the step shown in Fig. 10G of the third embodiment. In this modification, the steps up to the state shown in Fig. 12A are the same as in the third embodiment. As shown in Fig. 12A, the number of openings in the photoresist 42 formed on the polysilicon film 41 is larger than in the third embodiment.

That is, following the same procedure as in the third embodiment, the photoresist opening 43 is formed by forming an opening about 0.6 μm wide in a region for isolating the lower electrodes 48 of adjacent stacked capacitor cells to be described later. Also, the photoresist openings 44 are formed by forming openings about 0.25 μm wide in regions near the centers of the lower electrodes 48 to be formed. In this modification, substantially cylindrical photoresist

openings 53 are formed between the photoresist openings 43 and 44.

By using the photoresist 42 as a mask, the polysilicon film 41 is selectively removed by dry etching. Since the width of the photoresist openings 44 is made smaller than the half width of the photoresist openings 43 and 53, the supply of the etchant is reduced by a microloading effect when the polysilicon film 41 exposed in the photoresist openings 44 is etched. As a consequence, the etching rate is decreased in these portions.

That is, the progress in etching the polysilicon film 41 exposed in the photoresist openings 43 and 53 is faster than the progress in etching the polysilicon film 41 exposed in the photoresist openings 44. Accordingly, the polysilicon film 41 exposed in the photoresist openings 43 and 53 is removed first, and the underlying BPSG film 39 is exposed.

This dry etching is stopped when the BPSG film 39 is exposed in the photoresist openings 43 and 53. Consequently, the polysilicon film 41 is separated in the position of the photoresist opening 43, forming the lower electrodes 48 of the stacked capacitor cells. In the photoresist openings 53, the underlying BPSG film is exposed to form substantially cylindrical openings 54 in the lower electrodes 48. Also, in the positions of the photoresist openings 44, the polysilicon film 41 remains on the bottom surfaces to form recesses 49 in the lower electrodes 48. This state is shown in Fig. 12B.

Subsequently, a silicon nitride film about 30 Å thick is deposited on the entire surface by LPCVD and oxidized in

an oxygen atmosphere at about 850℃, thereby forming the dielectric film 45 made from an ONO film.

The polysilicon film 46 having a thickness of about 1,500 Å and serving as an upper electrode of the stacked capacitor cells is formed on the dielectric film 45 by CVD and patterned together with the dielectric film 45, thereby completing a stacked capacitor cell structure including the lower electrodes 48, the dielectric film 45, and the polysilicon film 46 as an upper electrode as shown in Fig. 12C.

Subsequently, as shown in Fig. 12D, the BPSG film 50 is formed on the entire surface and subjected to reflow, and the contact holes 47 are formed to expose portions of the drain regions 38. Thereafter, the aluminum alloy film 51 as a bit line is filled in the contact holes 47 and deposited on the BPSG film by sputtering. Finally, the aluminum alloy film 51 is patterned to complete a stacked capacitor cell structure DRAM as shown in Figs. 12E and 13.

In this modification, the capacitance of the dielectric film 45 made from an ONO film can be further increased by the substantially cylindrical openings 54 compared to the third embodiment. As a consequence, the capacitive coupling ratio can be increased.

Note that the etching rate controlled by the microloading effect can be increased or decreased by properly changing the diameter of the photoresist openings 53 in the above modification. For example, the diameter may be made smaller than in the above modification to set the same etching rate as the photoresist openings 44, and the polysilicon film 41 may be removed to the extent to which

the underlying field oxide film 39 is not exposed.

If this is the case, in the step shown in Fig. 12A, substantially cylindrical photoresist openings 55 having a smaller diameter are formed between the photoresist openings 43 and 44 as shown in Fig. 14A.

By using a photoresist 42 as a mask, the polysilicon film 41 is selectively removed by dry etching. Since the width of the photoresist openings 44 and 55 is made smaller than the half width of the photoresist opening 43, the supply of the etchant is reduced by the microloading effect when the polysilicon film 41 exposed in the photoresist openings 44 and 55 is etched. As a consequence, the etching rate is decreased in these portions.

That is, the progress in etching the polysilicon film 41 exposed in the photoresist opening 43 is faster than the progress in etching the polysilicon film 41 exposed in the photoresist openings 44 and 55. Accordingly, the polysilicon film 41 exposed in the photoresist opening 43 is removed first, and the underlying BPSG film 39 is exposed.

This dry etching is stopped when the BPSG film 39 is exposed in the photoresist opening 43. Consequently, the polysilicon film 41 is separated in the position of the photoresist opening 43, forming lower electrodes 48 of stacked capacitor cells. In the positions of the photoresist openings 44, the polysilicon film 41 remains on the bottom surfaces to form recesses 49 in the lower electrodes 48. Also, in the positions of the photoresist openings 55, the polysilicon film 41 remains on the bottom surfaces to form substantially cylindrical recesses 56 in the lower electrodes 48. This state is shown in Fig. 14B.

Subsequently, a silicon nitride film about 30 Å thick is deposited on the entire surface by LPCVD and oxidized in an oxygen atmosphere at about 850℃, thereby forming the dielectric film 45 made from an ONO film.

The polysilicon film 46 having a thickness of about 1,500 Å and serving as an upper electrode of the stacked capacitor cells is formed on the dielectric film 45 by CVD and patterned together with the dielectric film 45, thereby completing a stacked capacitor cell structure including the lower electrodes 48, the dielectric film 45, and the polysilicon film 46 as an upper electrode as shown in Fig. 14C.

Subsequently, as shown in Fig. 14D, the BPSG film 50 is formed on the entire surface and subjected to reflow, and the contact holes 47 are formed to expose portions of the drain regions 38. Thereafter, the aluminum alloy film 51 as a bit line is filled in the contact holes 47 and deposited on the BPSG film by sputtering. Finally, the aluminum alloy film 51 is patterned to complete a stacked capacitor cell structure DRAM as shown in Figs. 14E and 15.

Note that in the third embodiment, a photoresist 6 may also be formed after the surface of a polysilicon film 5 is planarized as in the second embodiment. If this is the case, recesses can be formed in lower electrodes of capacitors without using the microloading effect as in the second embodiment. Additionally, since photolithography is performed by forming the photoresist 6 on the planarized polysilicon film 5, the widths of the photoresist openings 43 and 44 can be set with higher controllability.

In the second and third embodiments, an element

isolation structure can be formed by a field shield structure or a trench element isolation structure.

In the first to third embodiments, a silicon oxide film or an ONO film is used as a dielectric film. However, a dielectric film is not restricted to these films. For example, a ferroelectric film may also be used.

If a ferroelectric film is used, the polysilicon film 5, 11 can be replaced with a film made of platinum, a titanium compound, a tungsten compound or a ruthenium compound. It may also be formed of a double layer structure in which a conductive film made of, for example, poly-silicon is provided under a platinum film.

Any material having a ferroelectric characteristic can be used as a material of the above-mentioned ferroelectric film. For example, PZT(lead zirconate titanate), PLZT(lead lanthanum zirconate titanate), barium titanate, palladium titanate, barium strontium titanate and bismuth titanate can be used as the material of the ferroelectric film. A dielectric film made of, for example, tantalic oxides or Ta_2O_5BSTO, which has a high dielectric constant of more than 50, can be used instead of the ferroelectric film.

The third embodiment described above may also be applied to a multivalue DRAM having three or more values. For example, methods of read and write to multivalue DRAMs are described in Japanese Patent Laid-Open No. 60-239994.

Furthermore, an insulating film including a silicon nitride film or an insulating film including a silicon oxide film and a silicon nitride film may be used as a charge storage film.

WHAT IS CLAIMED IS:

1. A semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate, comprising:

an island-like charge storage film formed across said element isolation structure and said element active region so as to be formed on said element active region through an insulating film,

said charge storage film having a recess in a surface on said element active region and a hole formed on said element isolation structure to reach said element isolation structure;

a dielectric film so formed as to cover the surface of said charge storage film including inner surfaces of said hole; and

a conductive film formed on said dielectric film.

2. A device according to claim 1, wherein said charge storage film and said conductive film function as a floating gate and a control gate, respectively, thereby constituting a semiconductor memory.

3. A device according to claim 1, wherein said charge storage film is formed on each of a plurality of element isolation regions, and adjacent charge storage films are separated from each other with a spacing not less than twice a width of said recess.

4. A device according to claim 1, wherein said element isolation structure is selected from the group consisting of a field oxide film formed by LOCOS, a trench type element isolation structure, and a field shield element isolation structure.

5. A device according to claim 1, wherein said dielectric film contains a material selected from the group consisting of a ferroelectric film and a high dielectric film, and

at least one of said charge storage film and said conductive film contains a material selected from the group consisting of a titanium compound, a tungsten compound, a ruthenium compound, and platinum.

6. A device according to claim 2, wherein said semiconductor memory is a multivalue nonvolatile memory which can store one among different store states represented by three values or more.

7. A device according to claim 1, wherein said charge storage film comprises a film selected from the group consisting of an insulating film including a silicon nitride film, an insulating film including a silicon oxide film and a silicon nitride film, and a conductive film.

8. A semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate, comprising:

an island-like charge storage film formed across said element isolation structure and said element active region so as to be formed on said element active region through an insulating film,

said charge storage film having a recess in a surface on said element active region and a hole formed on said element isolation structure to reach said element isolation structure; and

a conductive film formed on said charge storage film.

9. A device according to claim 8, wherein said charge

storage film comprises a film selected from the group consisting of an insulating film including a silicon nitride film, an insulating film including a silicon oxide film and a silicon nitride film, and a conductive film.

10. A semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate and having a transistor constituted by a gate electrode and a pair of impurity diffusion layers in said element active region, comprising:

an insulating interlayer formed on said semiconductor substrate including said transistor;

a first hole formed in said insulating interlayer and having a surface layer of said impurity diffusion layer as a bottom surface;

an island-like charge storage film electrically connected to one of said impurity diffusion layers through said first hole;

a second hole formed in said charge storage film and having a surface layer of said insulating interlayer as a bottom surface;

a dielectric film so formed as to cover a surface of said charge storage film including inner surfaces of said second hole; and

a conductive film formed on said dielectric film ,

wherein said charge storage film, said dielectric film, and said conductive film constitute a capacitor.

11. A device according to claim 10, wherein said dielectric film contains a material selected from the group consisting of a ferroelectric film and a high dielectric film, and

at least one of said charge storage film and said conductive film contains a material selected from the group consisting of a titanium compound, a tungsten compound, a ruthenium compound, and platinum.

12. A device according to claim 10, wherein said semiconductor device is a multivalue DRAM which can store one among different store states represented by three values or more.

13. A device according to claim 10, wherein said charge storage film comprises a film selected from the group consisting of an insulating film including a silicon nitride film, an insulating film including a silicon oxide film and a silicon nitride film, and a conductive film.

14. A semiconductor device including an element active region defined by forming an element isolation structure on a semiconductor substrate, comprising:

an insulating film formed on said semiconductor substrate in said element active region; and

a charge storage film patterned on said insulating film,

wherein said charge storage film is formed across said element isolation structure and has a hole on said element isolation structure, and

at least a portion of a bottom surface of said hole reaches a surface layer of said element isolation structure.

15. A device according to claim 14, wherein said element isolation structure is selected from the group consisting of an element isolation structure made from an insulating film and an element isolation structure

including an electrode for isolation.

16. A device according to claim 14, further comprising:

a dielectric film formed on said charge storage film including inner surfaces of said hole; and

a conductive film formed on said dielectric film.

17. A device according to claim 14, wherein said charge storage film functions as a floating gate of a nonvolatile transistor.

18. A device according to claim 16, wherein said dielectric film contains a material selected from the group consisting of a ferroelectric film and a high dielectric film, and

at least one of said charge storage film and said conductive film contains a material selected from the group consisting of a titanium compound, a tungsten compound, a ruthenium compound, and platinum.

19. A device according to claim 14, wherein said semiconductor device is a multivalue memory which can store one among different store states represented by three values or more.

20. A device according to claim 14, wherein said charge storage film comprises a film selected from the group consisting of an insulating film including a silicon nitride film, an insulating film including a silicon oxide film and a silicon nitride film, and a conductive film.

21. A semiconductor device including a plurality of element isolation regions defined by forming an element isolation structure on a semiconductor substrate, comprising:

an island-like charge storage film formed across said

element isolation structure and said element active regions and having a recess;

a dielectric film so formed as to cover a surface of said charge storage film; and

a conductive film formed on said dielectric film and capacitively coupled with said charge storage film,

wherein said charge storage film is formed in each of said element active regions, and an upper surface of each of said charge storage films is planarized by CMP and flush with an upper surface of an adjacent charge storage film.

22. A device according to claim 21, wherein said element isolation structure is selected from the group consisting of a field oxide film formed by LOCOS, a trench type element isolation structure, and a field shield element isolation structure.

23. A device according to claim 21, wherein a hole reaching said element isolation structure is formed in a portion of said charge storage film above said element isolation structure.

24. A device according to claim 21, wherein a bottom surface of said recess is substantially flush with or lower than a surface of said element isolation structure.

25. A device according to claim 21, wherein said dielectric film contains a material selected from the group consisting of a ferroelectric film and a high dielectric film, and

at least one of said charge storage film and said conductive film contains a material selected from the group consisting of a titanium compound, a tungsten compound, a ruthenium compound, and platinum.

26. A device according to claim 21, wherein said charge storage film and said conductive film function as a floating gate and a control gate, respectively, thereby constituting a semiconductor memory.

27. A device according to claim 21, wherein said charge storage film comprises a film selected from the group consisting of an insulating film including a silicon nitride film, an insulating film including a silicon oxide film and a silicon nitride film, and a conductive film.

28. A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming an insulating film on said semiconductor substrate in said element active region;

the third step of forming a first conductive film on an entire surface of said semiconductor substrate including said insulating film and said element isolation structure;

the fourth step of forming a mask pattern having first and second openings on said first conductive film;

the fifth step of etching said first conductive film until said element isolation structure is exposed in said first opening by using said mask pattern as a mask, thereby dividing said first conductive film, and simultaneously forming a recess in said second opening by leaving said first conductive film behind on a bottom;

the sixth step of forming a dielectric film so as to cover a surface of said first conductive film; and

the seventh step of forming a second conductive film on

said dielectric film and opposing said second conductive film to said first conductive film through said dielectric film.

29. A method according to claim 28, further comprising, after the seventh step, the eighth step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said first conductive film.

30. A method according to claim 28, wherein in the fourth step, said mask pattern is so formed that a width of said first opening is not less than twice a width of said second opening.

31. A method according to claim 28, further comprising, between the third and fourth steps, the ninth step of planarizing said first conductive film by polishing, and

wherein in the fourth step, said mask pattern is so formed that said second opening is positioned above said element active region.

32. A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate insulating film and a gate electrode in said element active region;

the third step of doping an impurity into said second substrate to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming a first conductive film electrically connected to one of said impurity diffusion layers;

the fifth step of forming a mask pattern having at least first and second openings on said first conductive film;

the sixth step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film in said first opening, and simultaneously forming a recess in said second opening by leaving said first conductive film behind on a bottom;

the seventh step of forming a dielectric film so as to cover a surface of said first conductive film; and

the eighth step of forming a second conductive film on said dielectric film and opposing said second conductive film to said first conductive film through said dielectric film.

33. A method according to claim 32, further comprising, between the third and fourth steps,

the ninth step of forming an insulating interlayer on an entire surface of said semiconductor substrate, and

the 10th step of forming a hole in said insulating interlayer in which one of said impurity diffusion layers is exposed, and

wherein in the fourth step, a first conductive film is formed on said insulating interlayer and said hole is filled with said first conductive film, and

in the sixth step, said first conductive film is etched until said insulating interlayer is exposed in said first opening.

34. A method according to claim 32, wherein in the seventh step, said mask pattern is so formed that a width of said first opening is not less than twice a width of said second opening.

35. A method according to claim 32, further comprising, between the fourth and fifth steps, the 11th step of planarizing said first conductive film by polishing, and

wherein in the fifth step, said mask pattern is so formed that said second opening is positioned above said element active region.

36. A method of fabricating a semiconductor device, comprising:

the first step of forming a first conductive film in an insulating film region on a semiconductor substrate;

the second step of forming a mask pattern having two types of openings on said first conductive film;

the third step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film conforming to a shape of one of said openings and simultaneously forming at least one recess in a surface of said divided first conductive film conforming to a shape of the other opening;

the fourth step of forming an insulating film so as to cover a surface of said first conductive film; and

the fifth step of forming a second conductive film so as to cover a surface of said insulating film and opposing said second conductive film to said first conductive film through said insulating film.

37. A method according to claim 36, wherein in the third step, said recess is so formed as to reach said

insulating film region, thereby forming a hole in which a surface of said insulating film region is exposed.

38. A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming an insulating film on said semiconductor substrate in said element active region;

the third step of forming a first conductive film on an entire surface including said insulating film and said element isolation structure;

the fourth step of forming a mask pattern having at least first and second openings on said first conductive film;

the fifth step of etching said first conductive film until said element isolation structure is exposed in said first and second openings by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a hole extending through said first conductive film below said second opening;

the sixth step of forming a dielectric film so as to cover said first conductive film; and

the seventh step of forming a second conductive film on said dielectric film and opposing said second conductive film to said first conductive film through said dielectric film.

39. A method according to claim 38, further comprising, after the seventh step, the eight step of doping an

impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said first conductive film.

40. A method according to claim 38, further comprising, between the third and fourth steps, the ninth step of planarizing said first conductive film by polishing.

41. A method according to claim 38, wherein in the first step, a field shield element isolation structure in which a shield plate electrode is embedded is formed on said semiconductor substrate.

42. A method of fabricating a semiconductor substrate, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate oxide film and a gate electrode on said semiconductor substrate in said element active region;

the third step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming a first conductive film electrically connected to one of said impurity diffusion layers;

the fifth step of forming a mask pattern having at least first and second openings on said first conductive film;

the sixth step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a hole extending through said first conductive film below said second opening;

the seventh step of forming a dielectric film so as to cover a surface of said first conductive film; and

the eighth step of forming a second conductive film so as to cover said dielectric film and opposing said second conductive film to said first conductive film through said dielectric film.

43. A method according to claim 42, further comprising, between the third and fourth steps,

the ninth step of forming an insulating interlayer on an entire surface of said semiconductor substrate, and

the 10th step of forming a hole in said insulating interlayer in which one of said impurity diffusion layers is exposed, and

wherein in the fourth step, a first conductive film is formed on said insulating interlayer and said hole is filled with said first conductive film, and

in the sixth step, said first conductive film is etched until said insulating interlayer is exposed in said first and second openings.

44. A method according to claim 42, further comprising, between the fourth and fifth steps, the ninth step of planarizing said first conductive film by polishing.

45. A method according to claim 42, wherein in the first step, a field shield element isolation structure in which a shield plate electrode is embedded is formed on said

Fig.1A

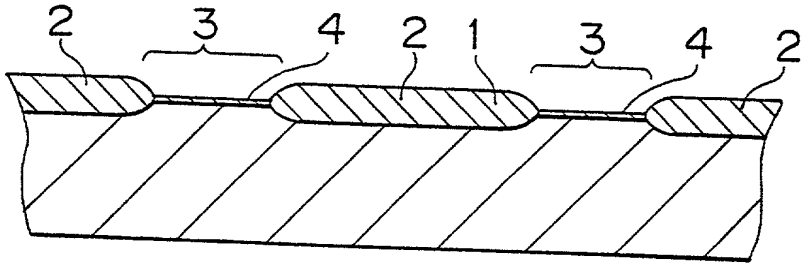

Fig.1B

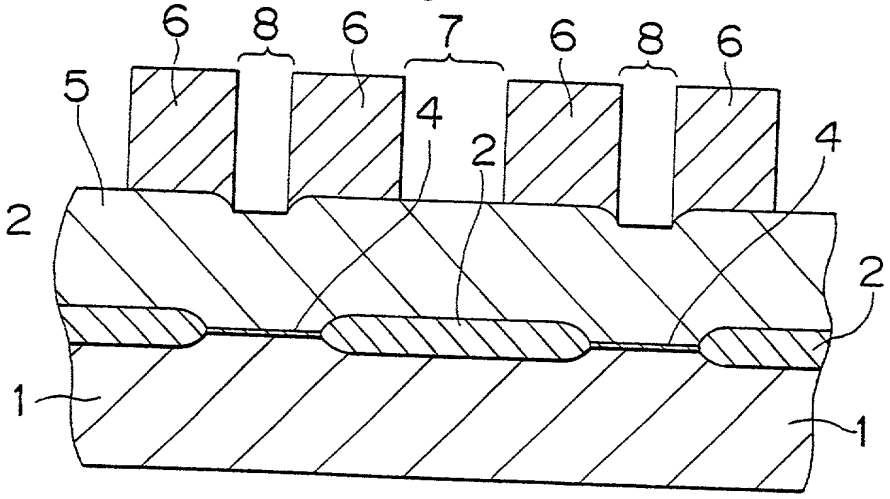

Fig.1C

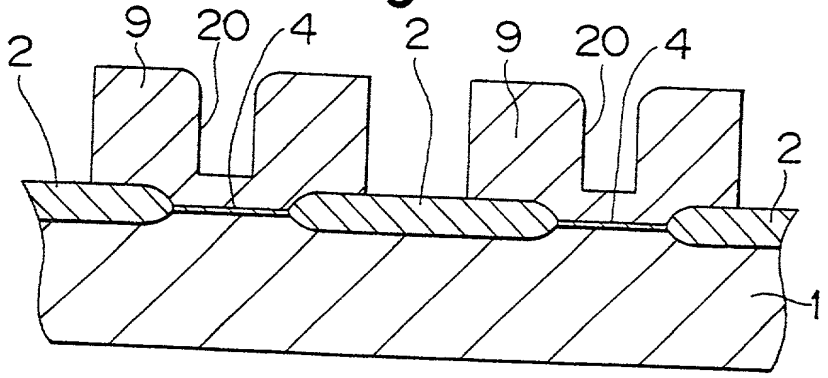

Fig.1D

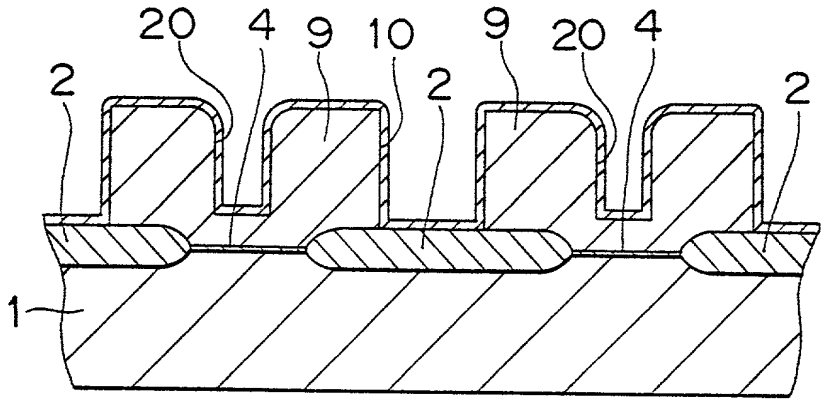

Fig.1E

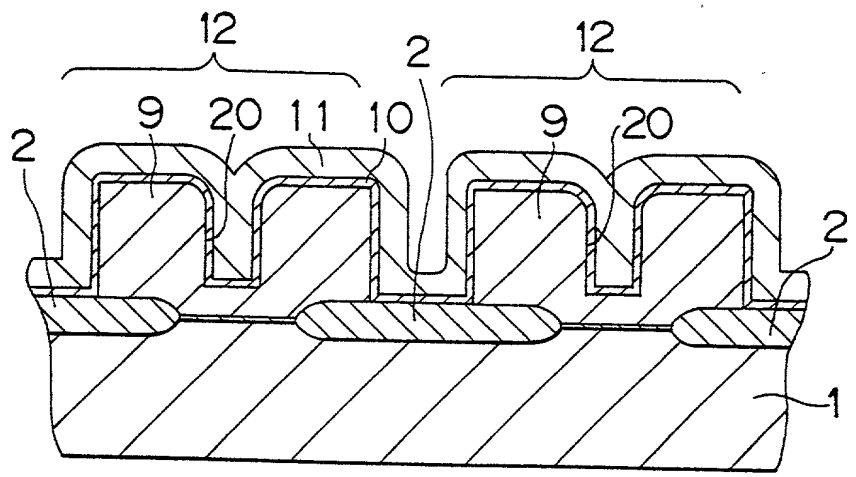

Fig.1F

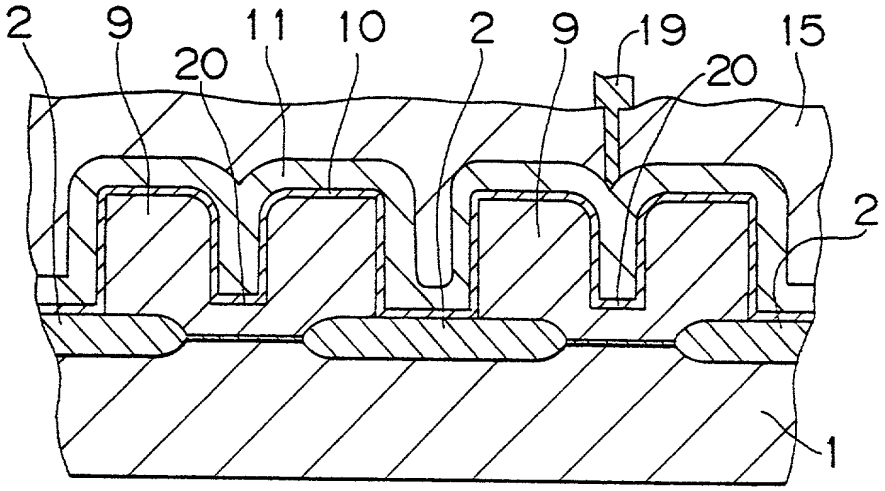

Fig.1G

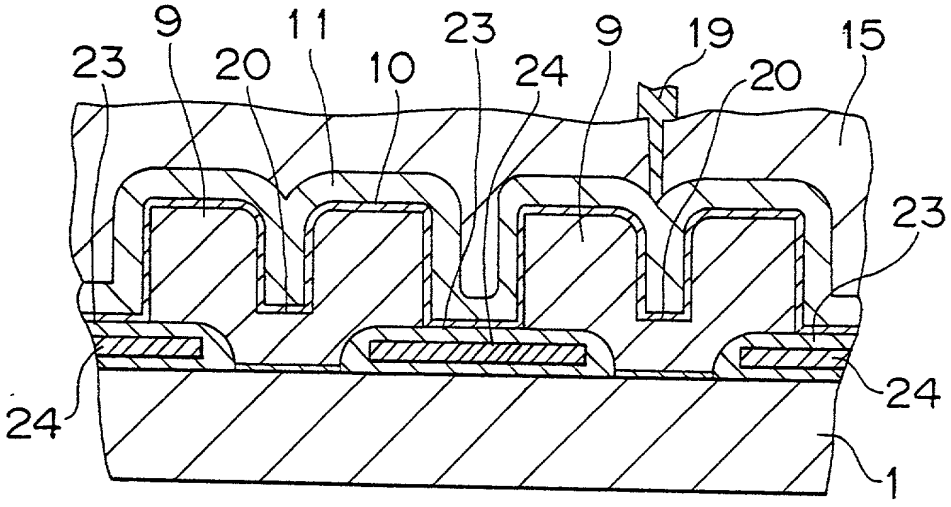

Fig.2A

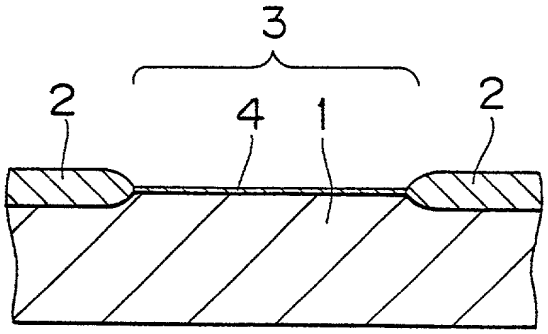

Fig.2B

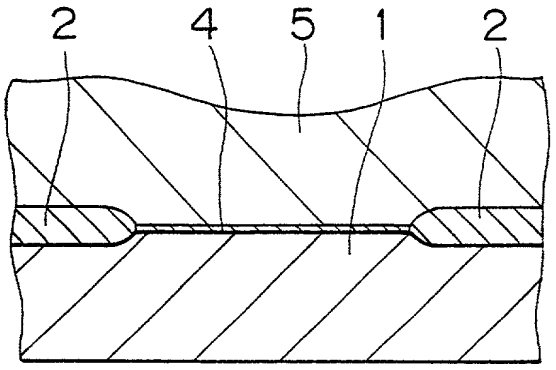

Fig.2C

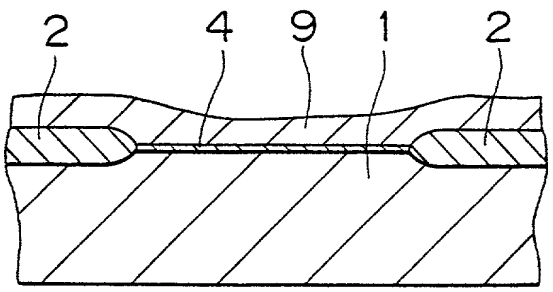

Fig.2D

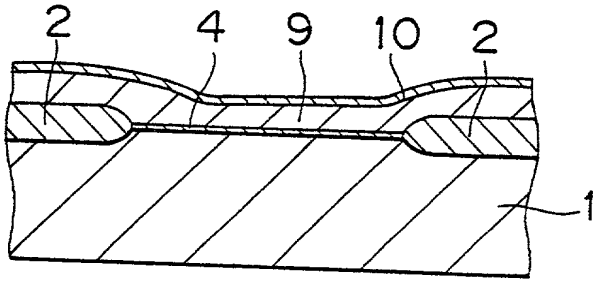

Fig.2E

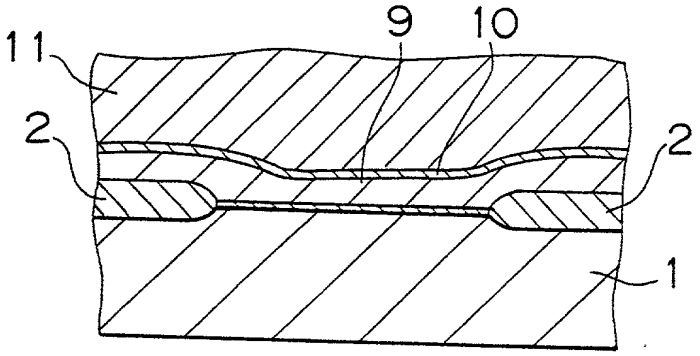

Fig.2F

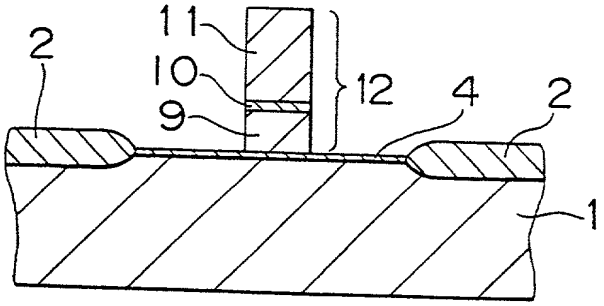

Fig.2G

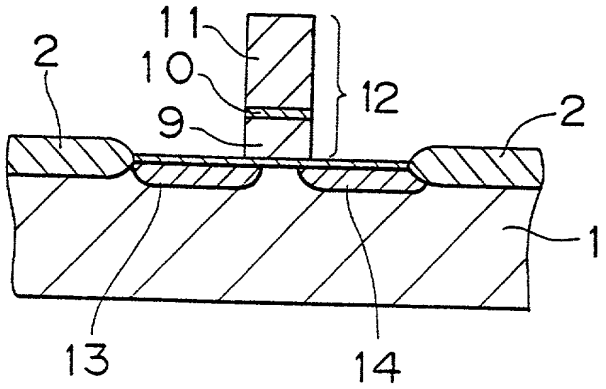

Fig.2H

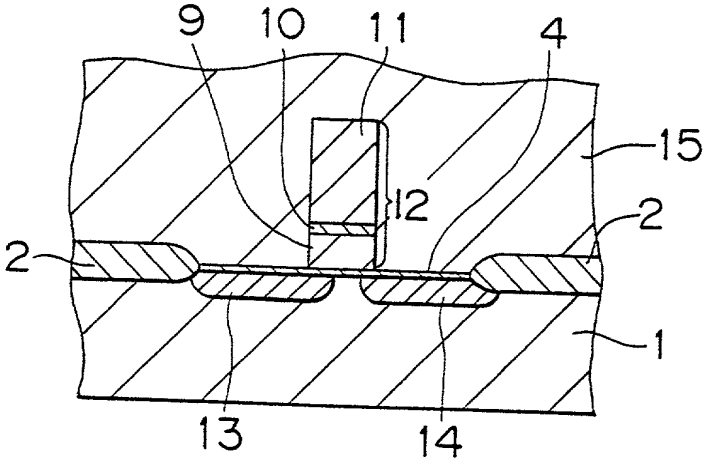

Fig.2I

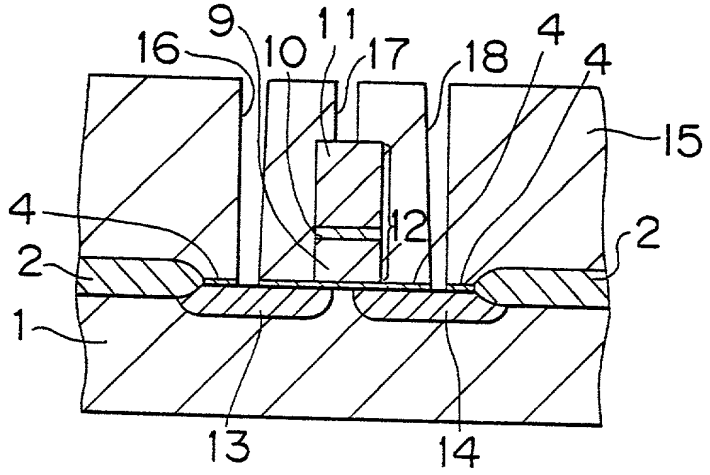
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Fig.2J

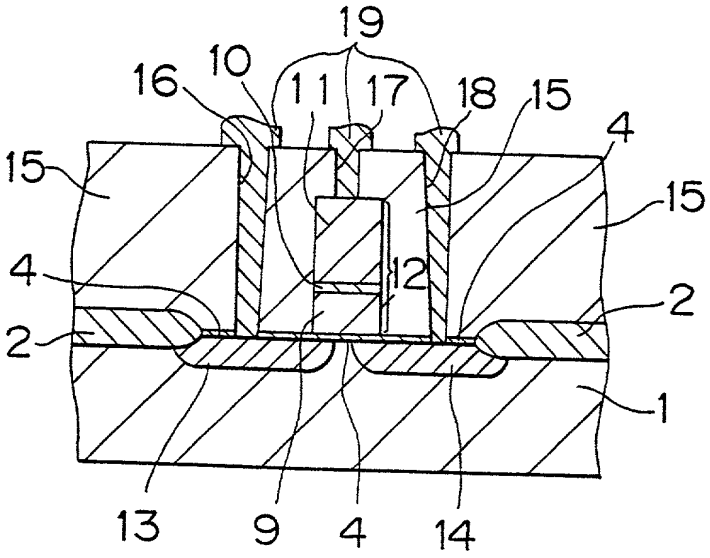
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Fig.3

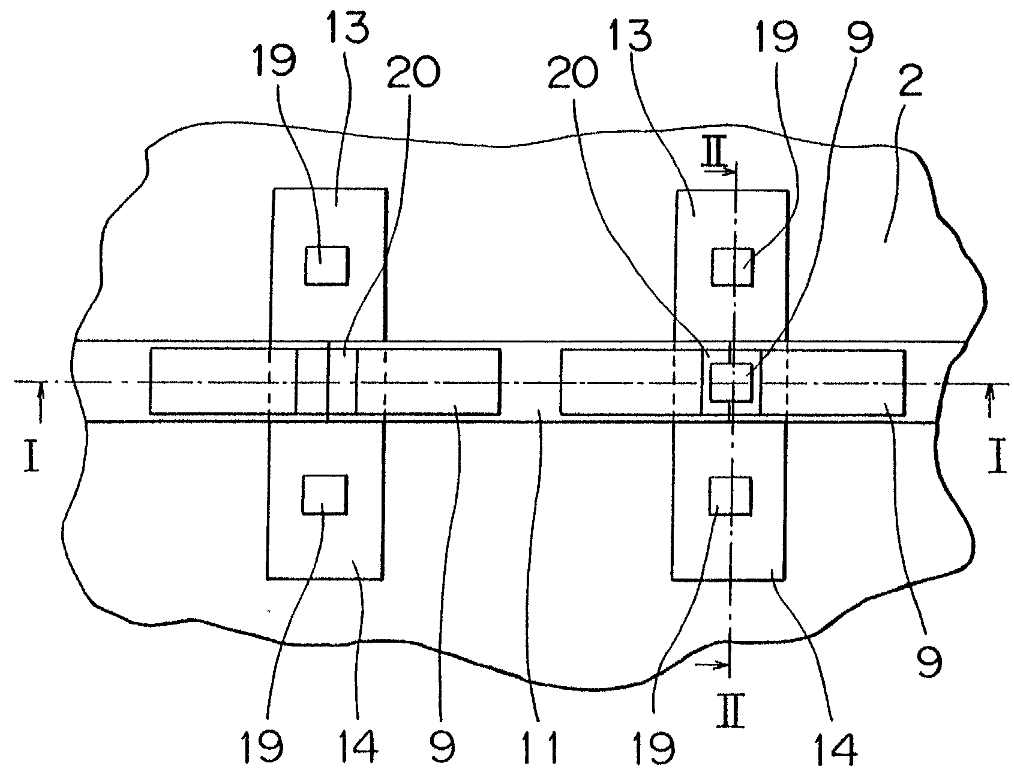

Fig.4A

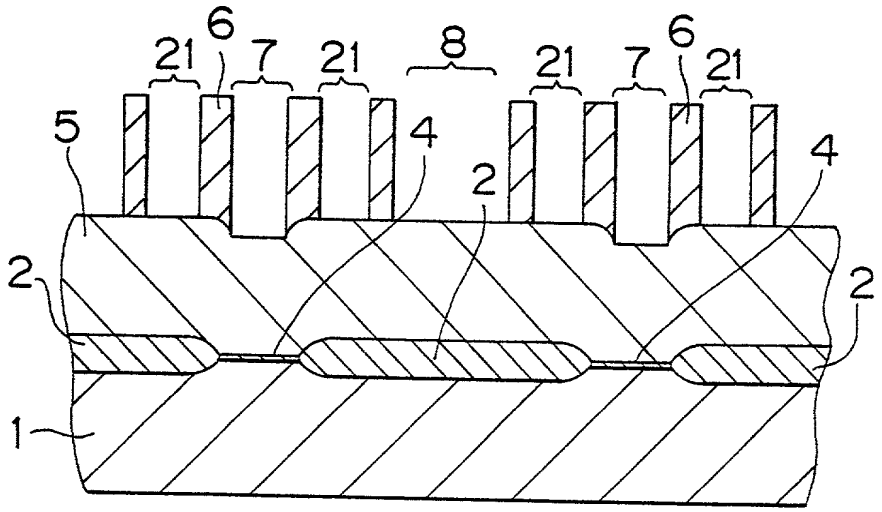

Fig.4B

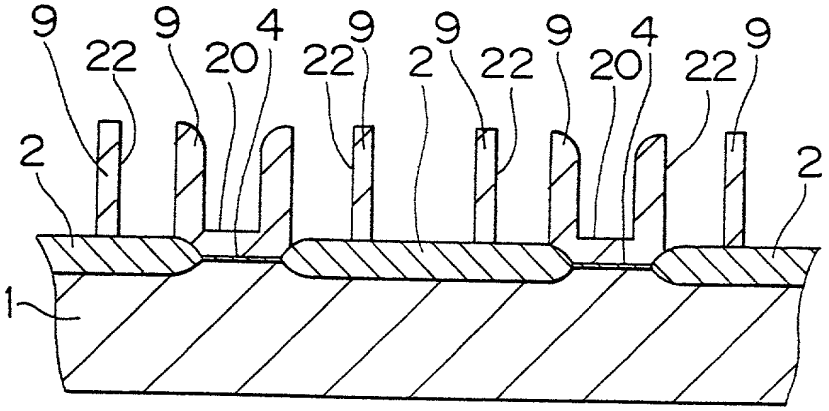

Fig.4C

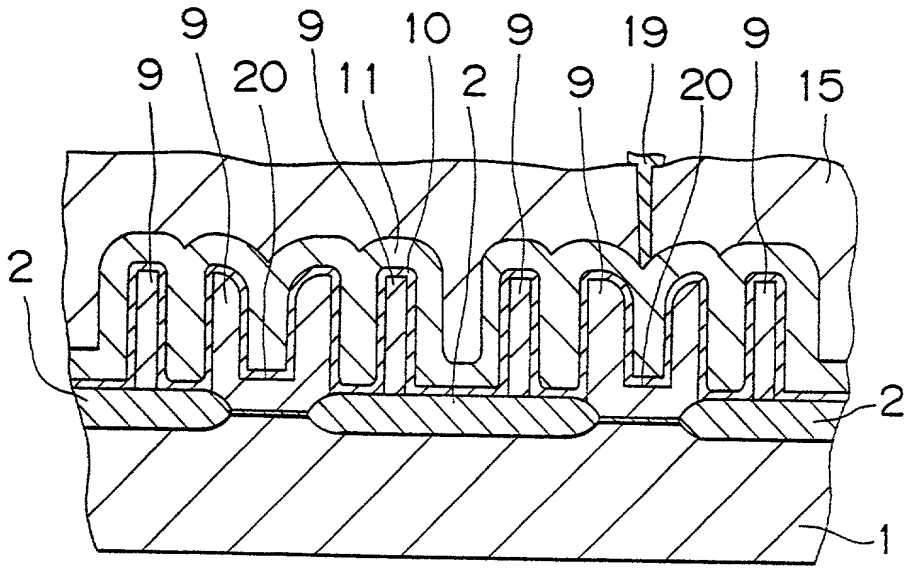

Fig.5

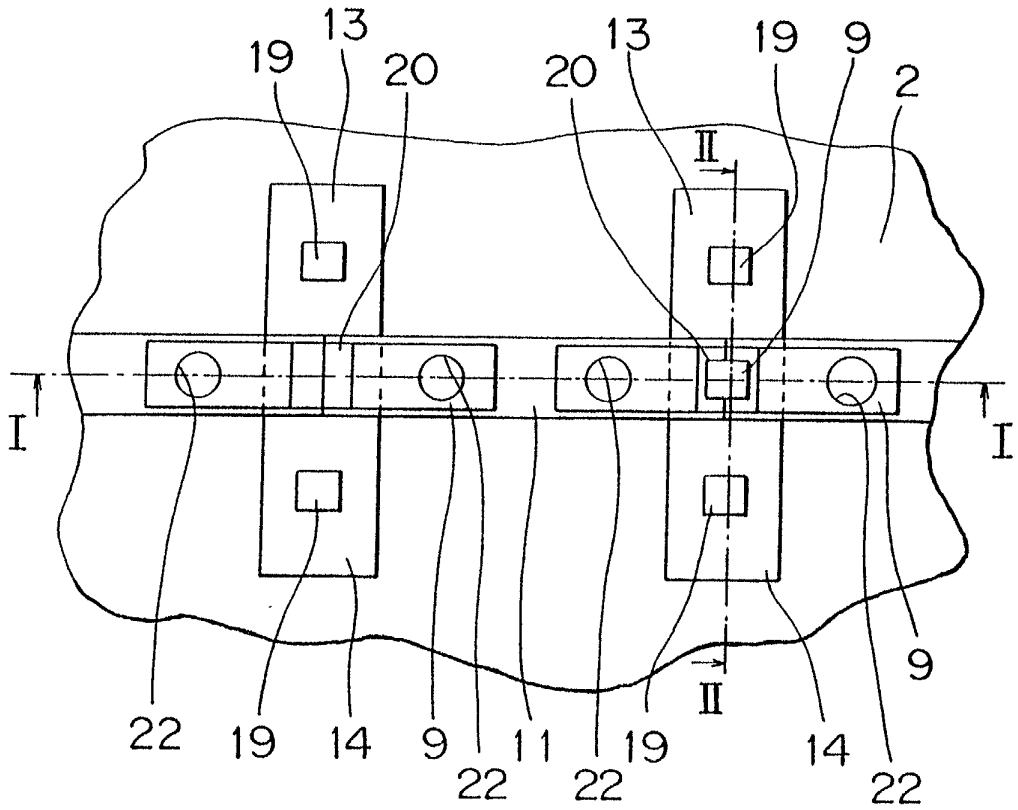

Fig.6A

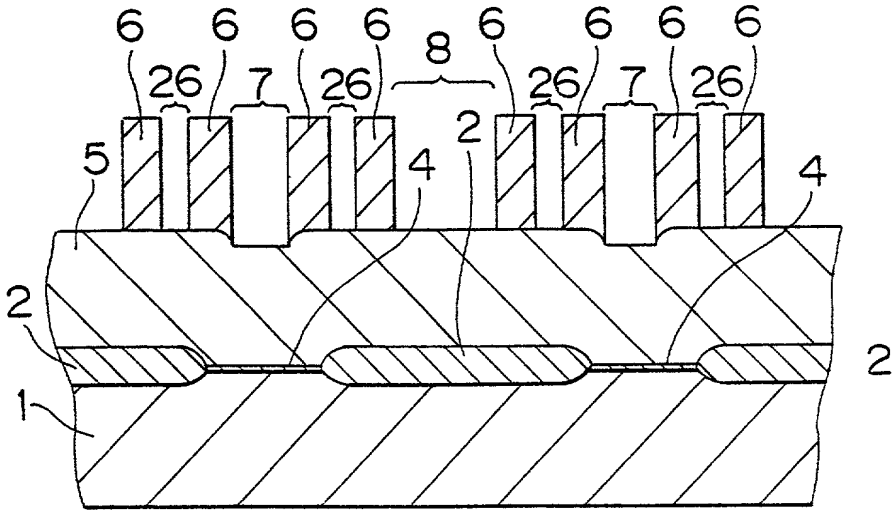

Fig.6B

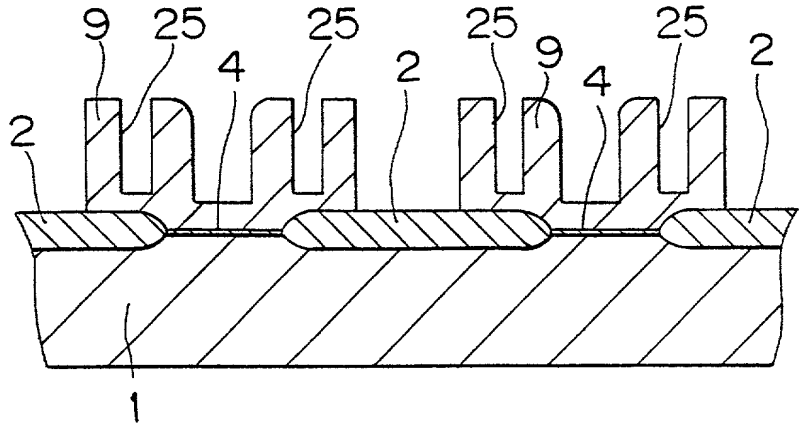

Fig.6C

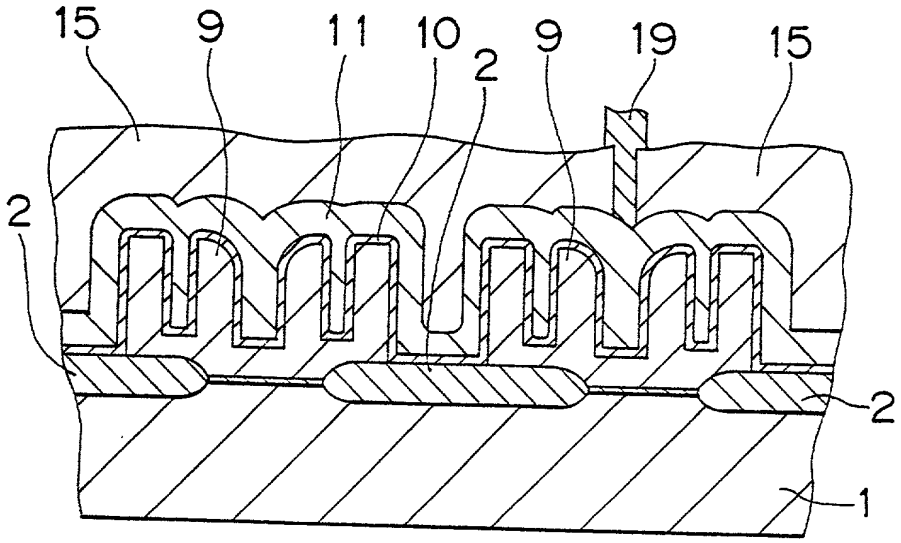

Fig.10J

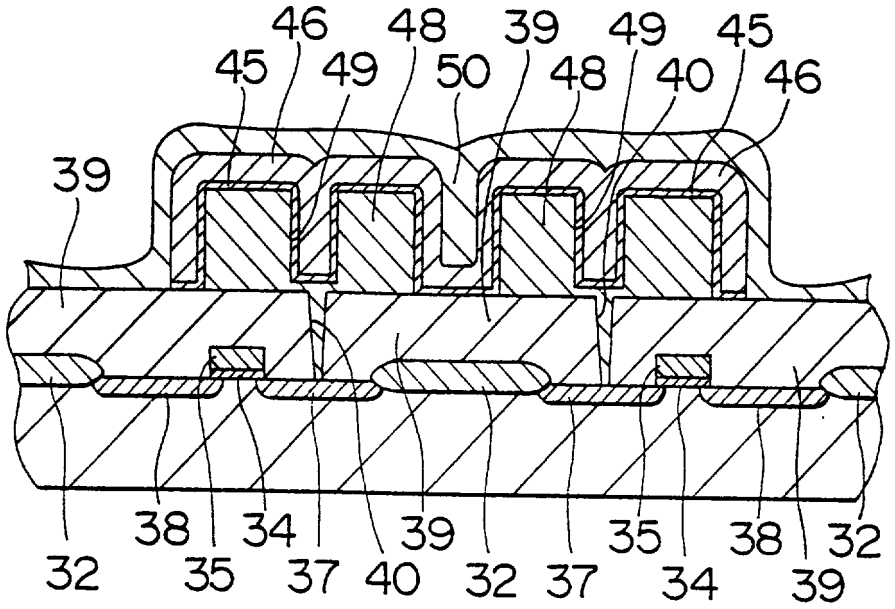

Fig.10K

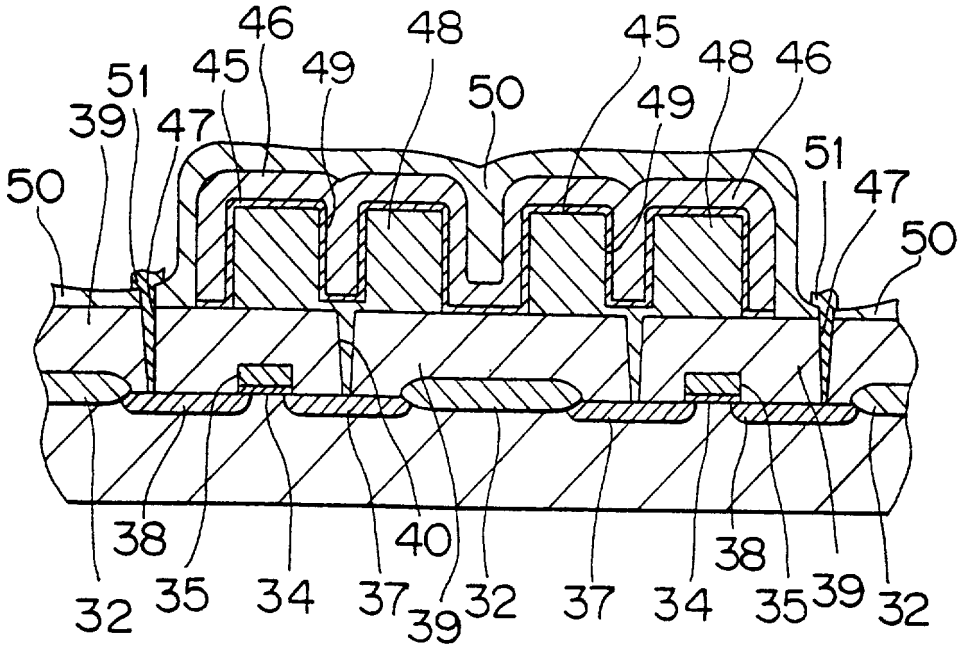

Fig.7

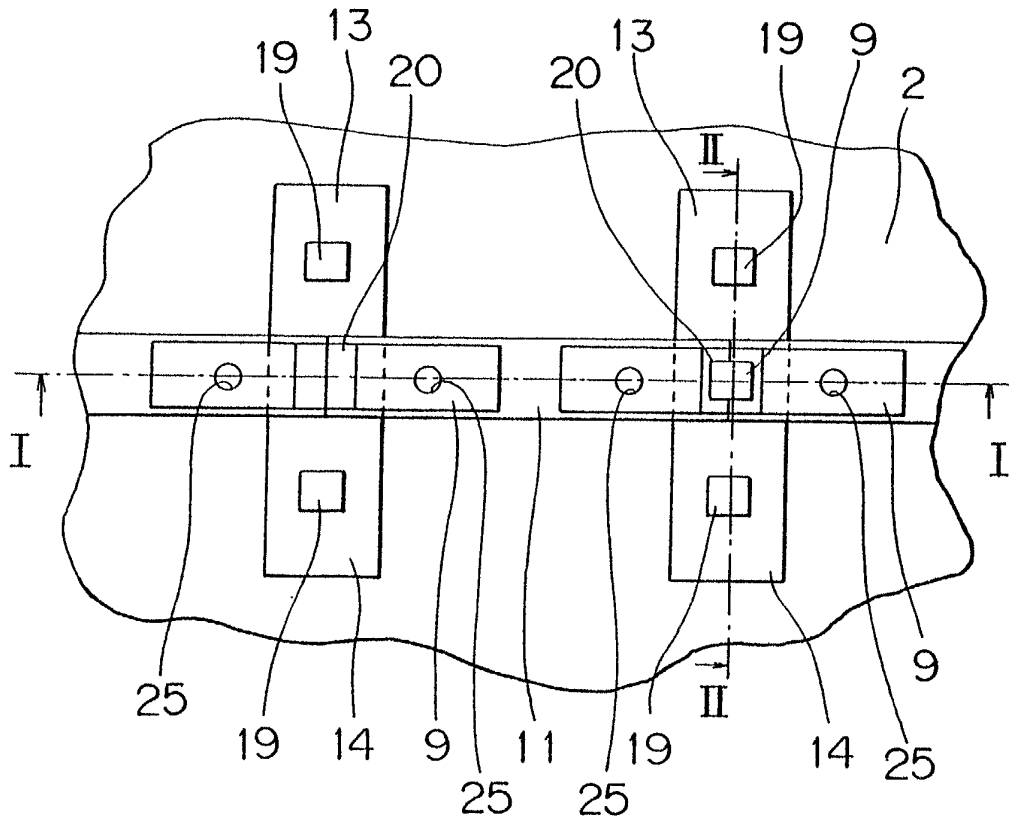

Fig.8A

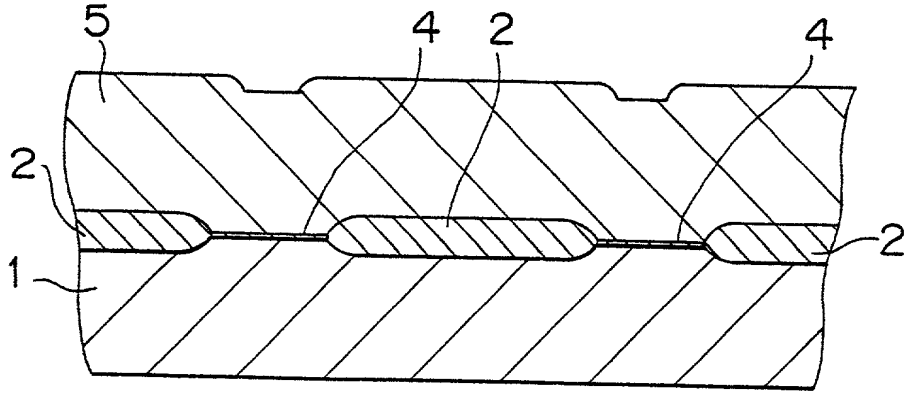

Fig.8B

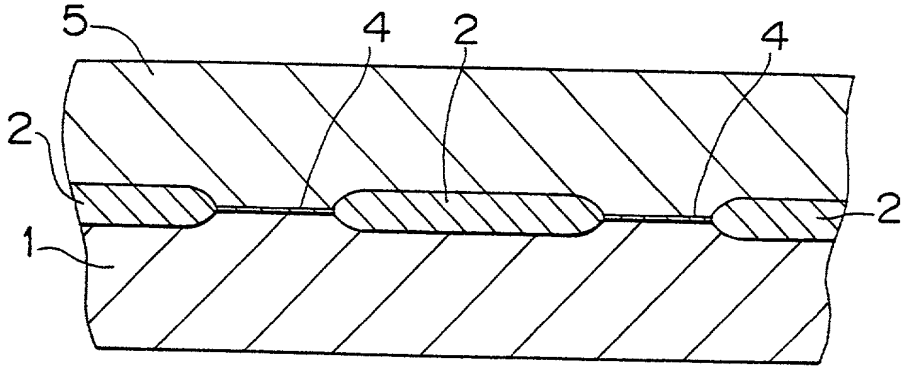

Fig.8C

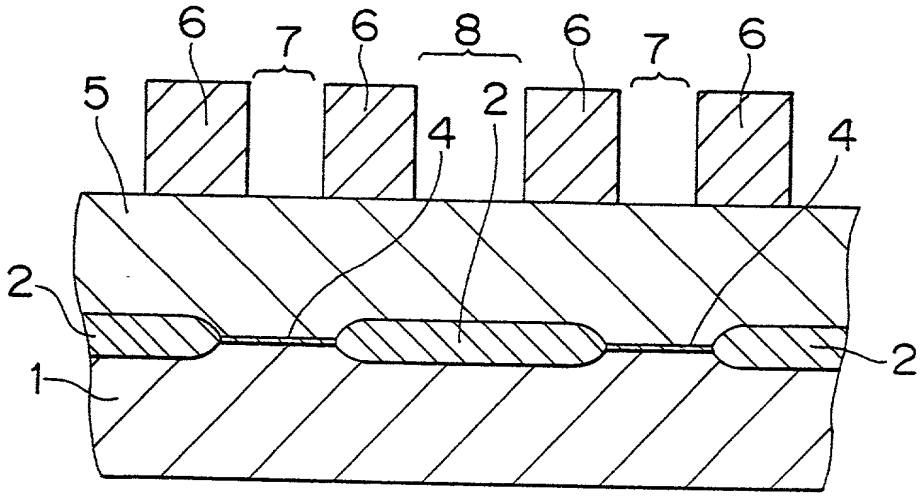

Fig.8D

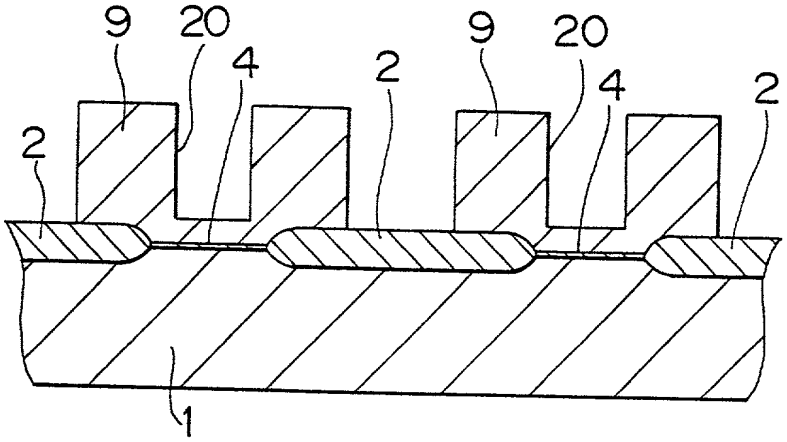

Fig.9

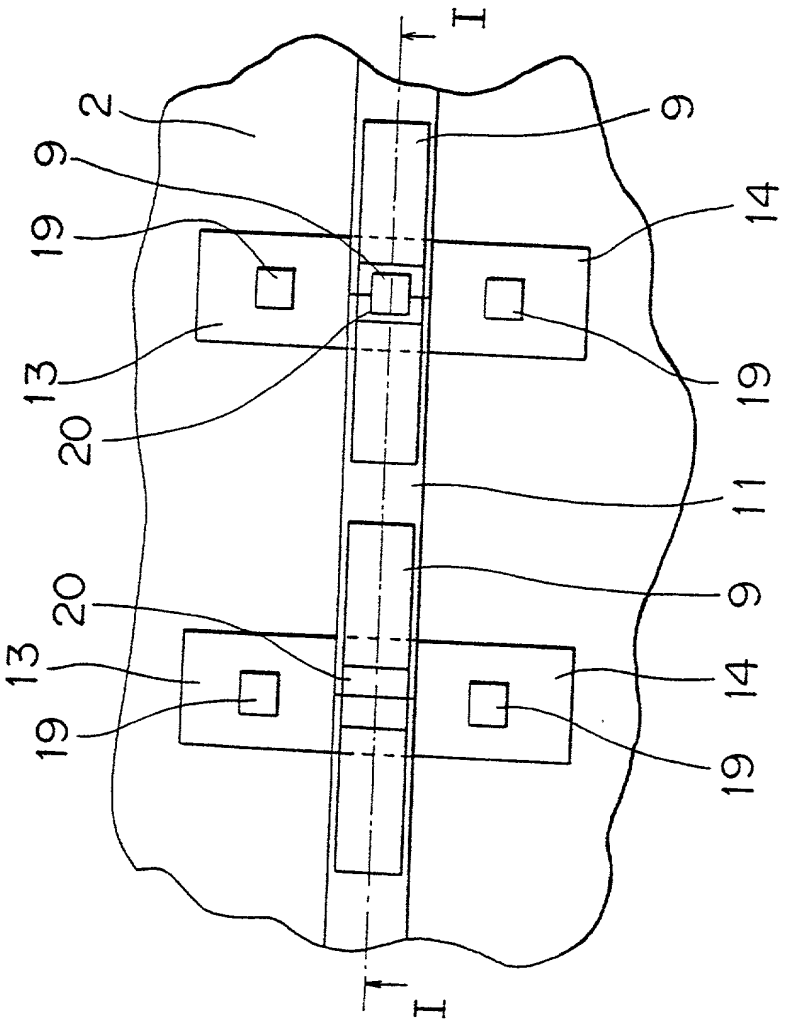

Fig.10A

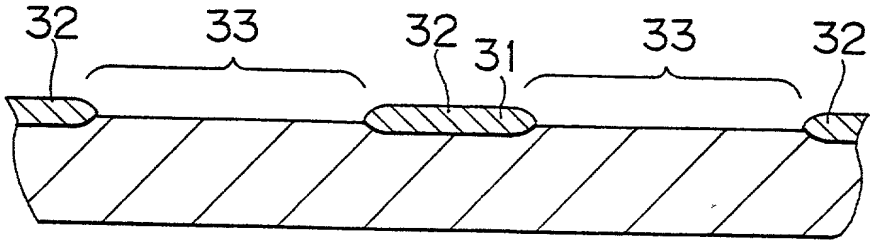

Fig.10B

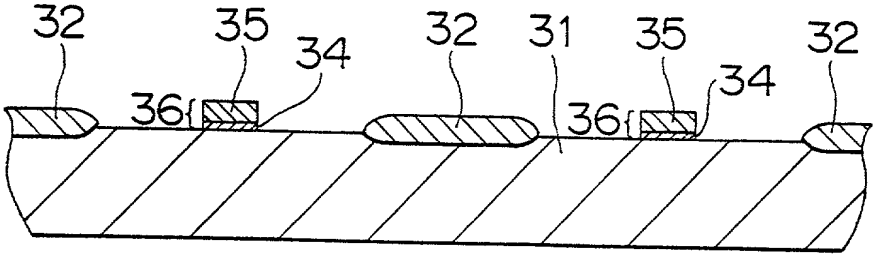

Fig.10C

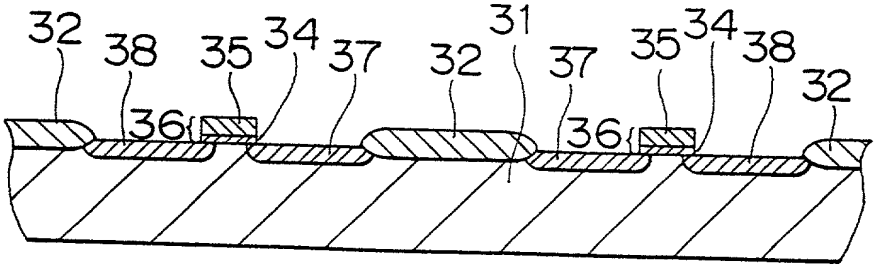

Fig.10D

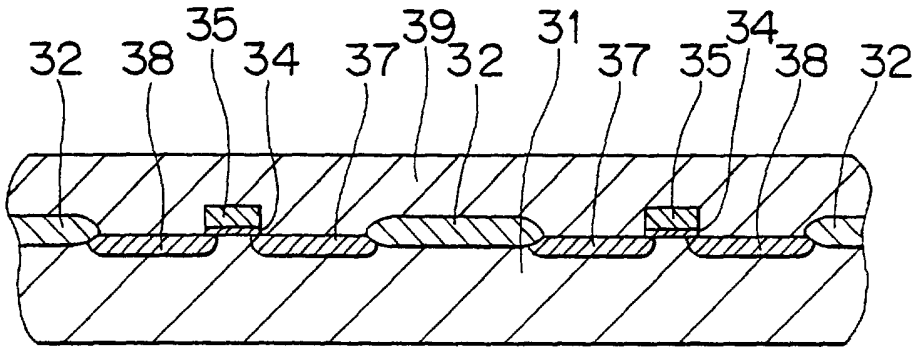

Fig.10E

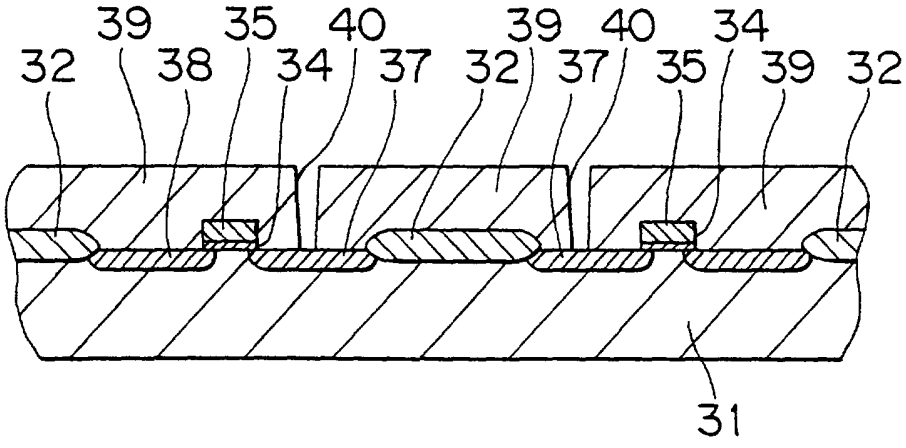

Fig.10F

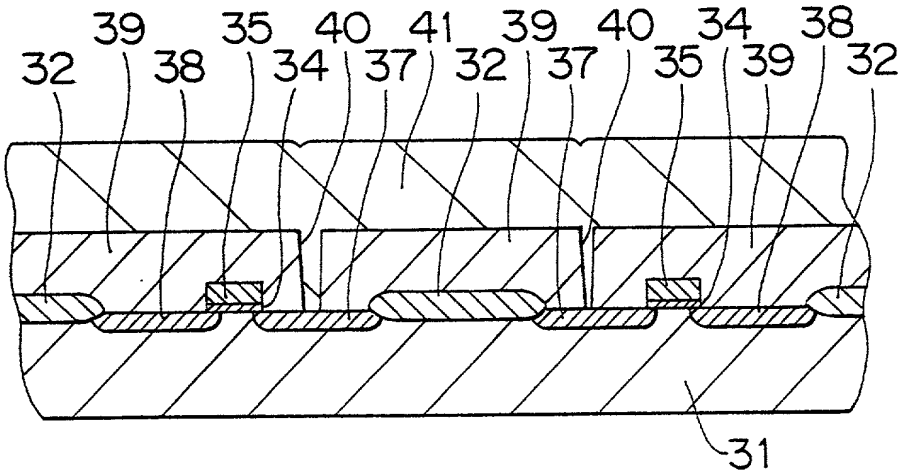

Fig.10G

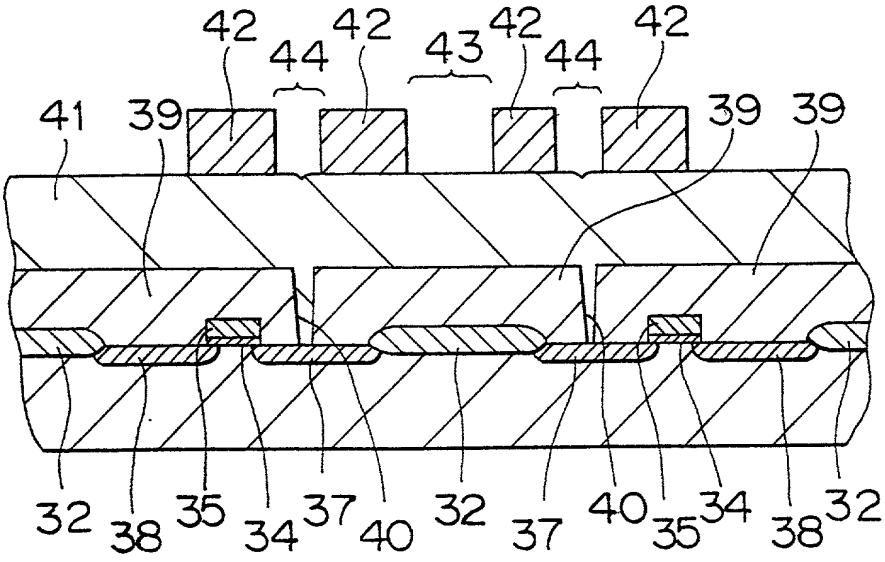

Fig.10H

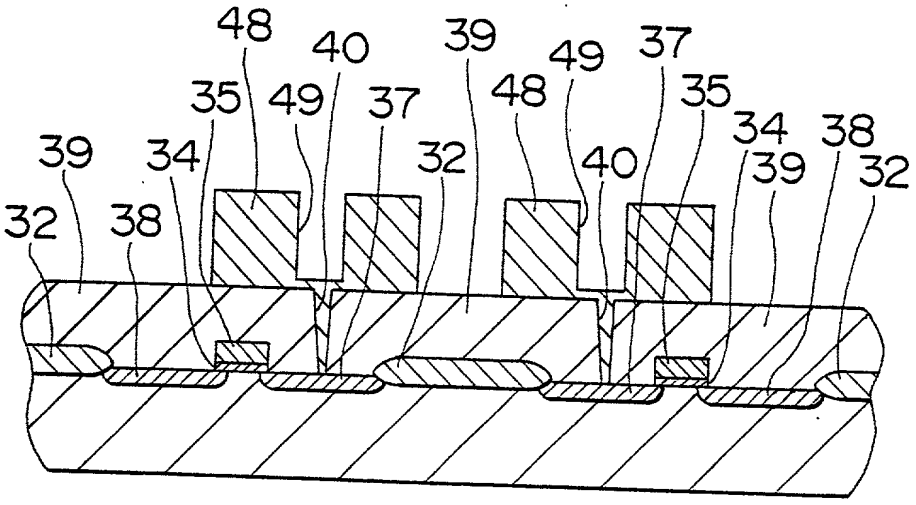

Fig.10I

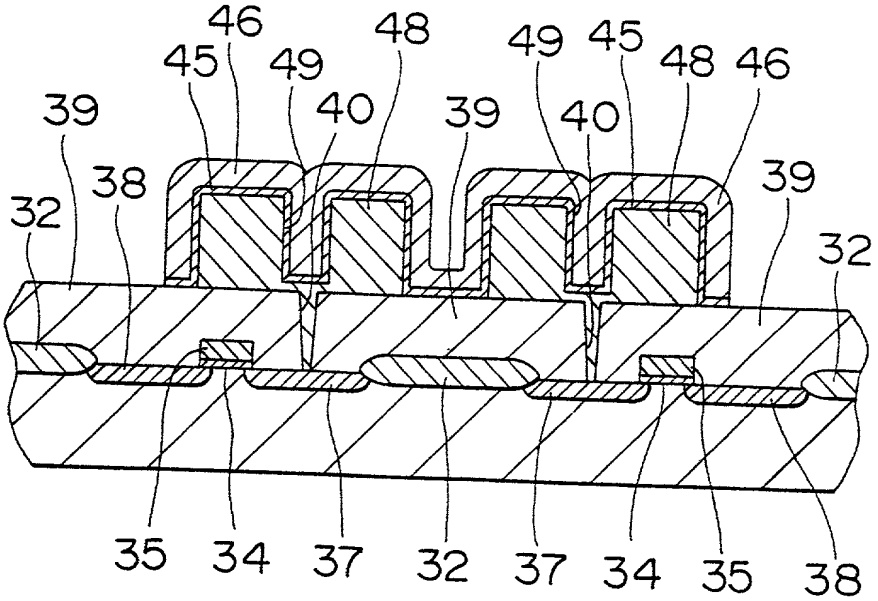

Fig.10J

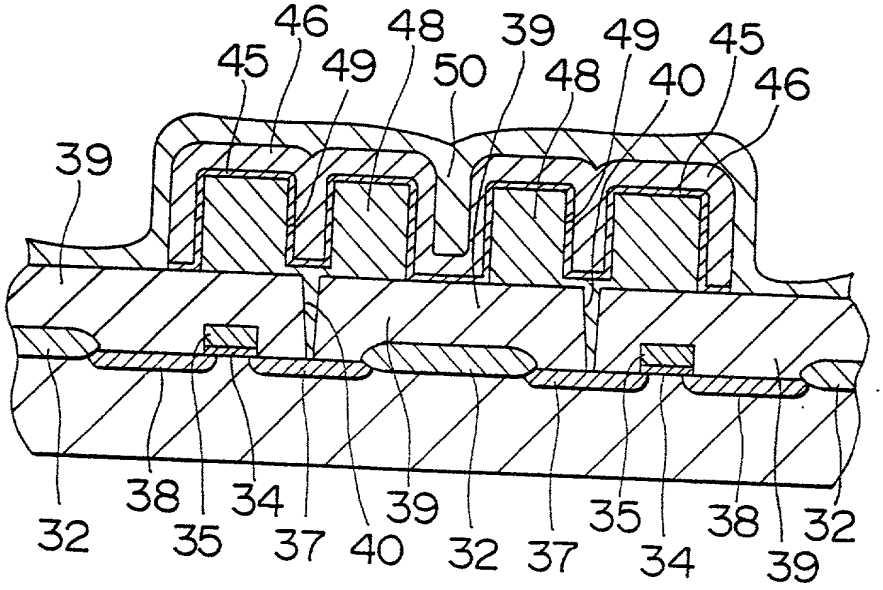

Fig.10K

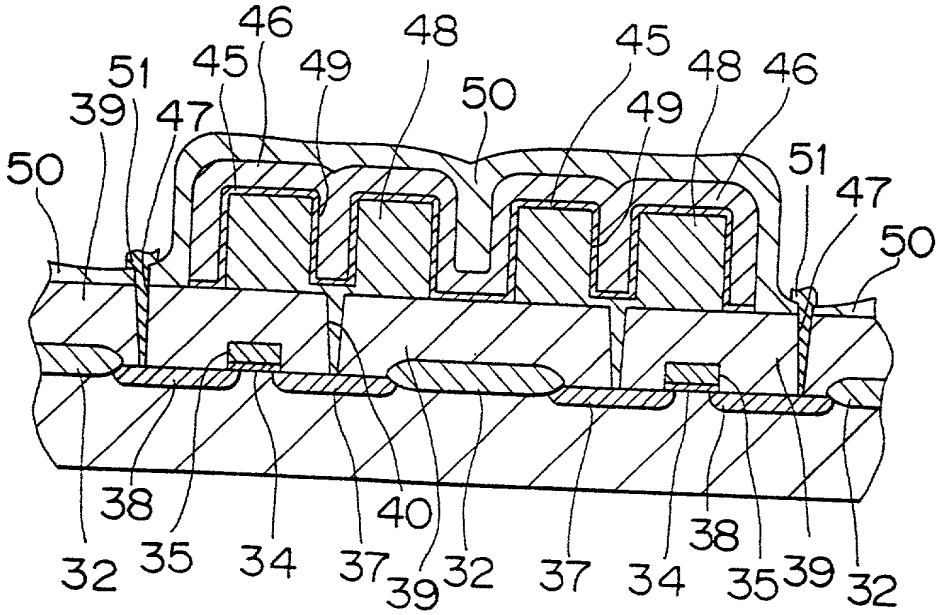

Fig.11

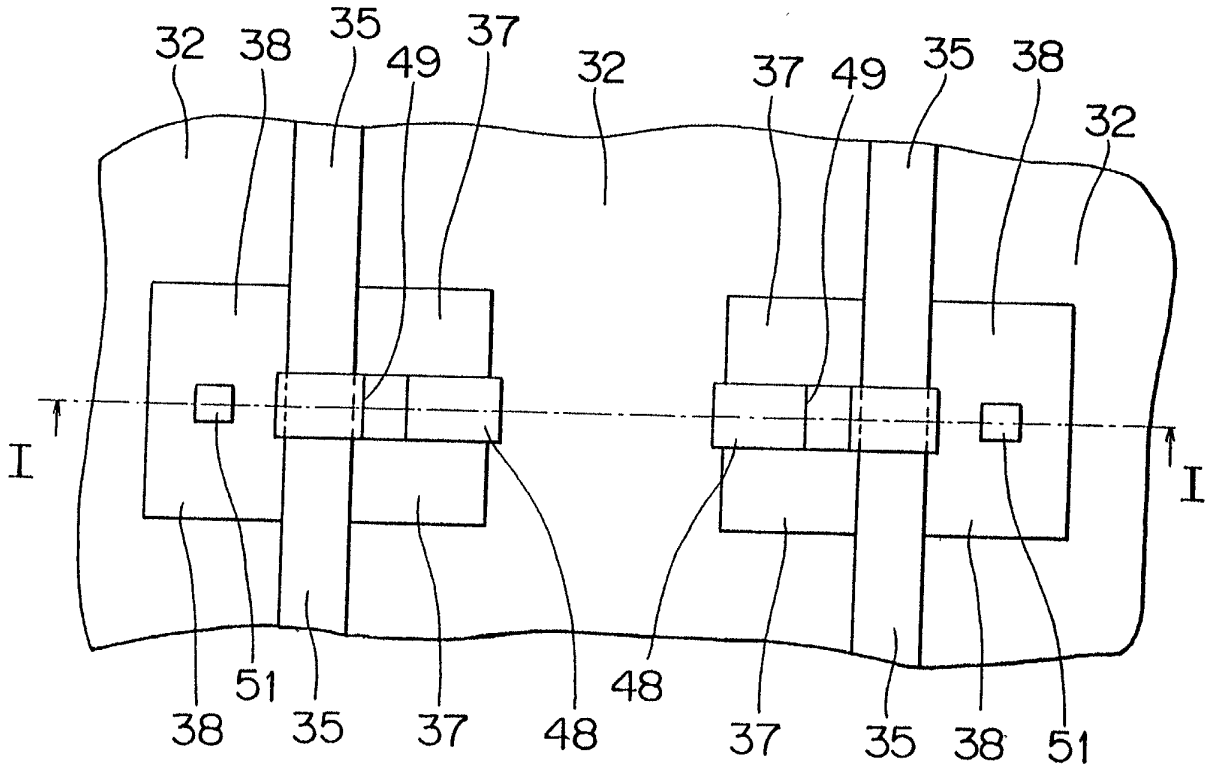

Fig.12A

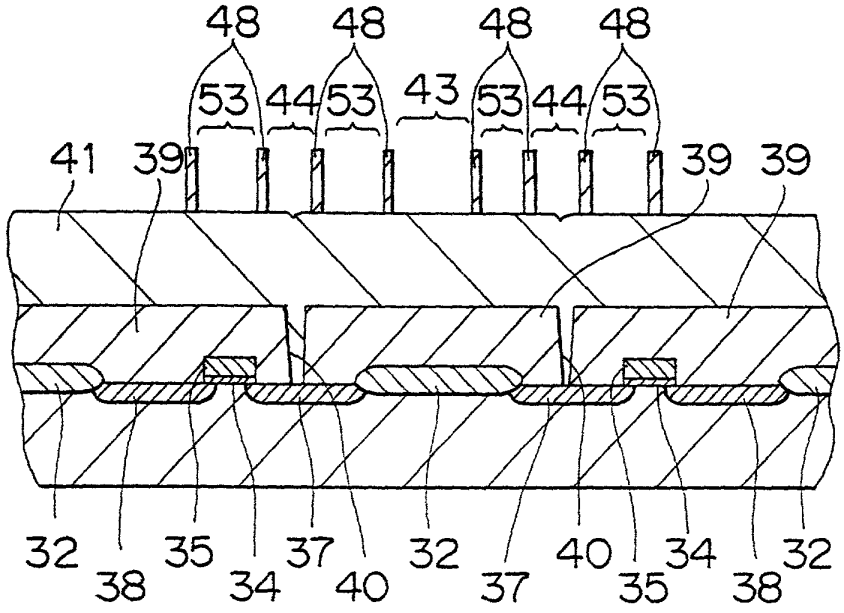

Fig.12B

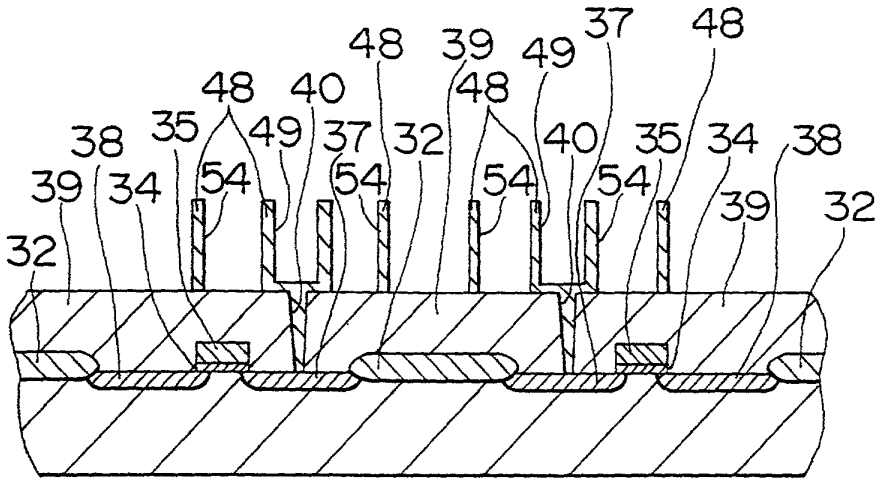

Fig.12C

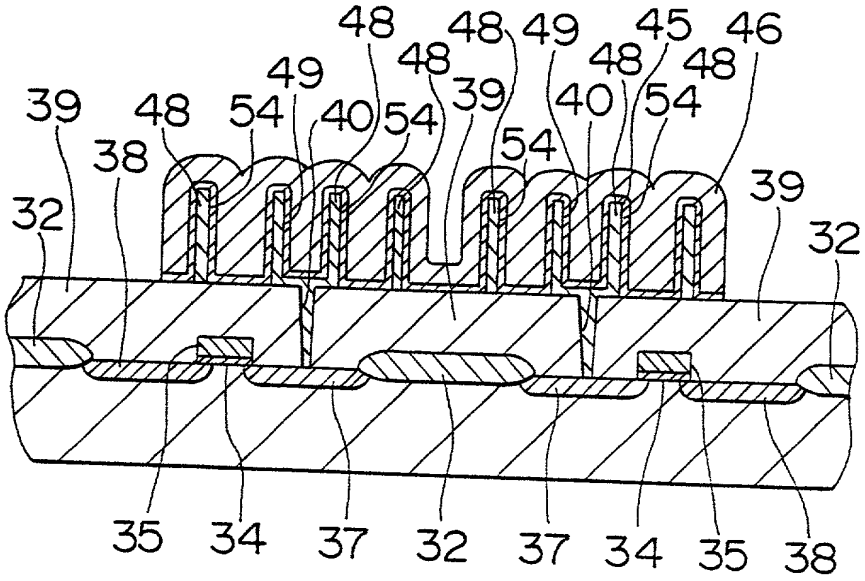

Fig.12D

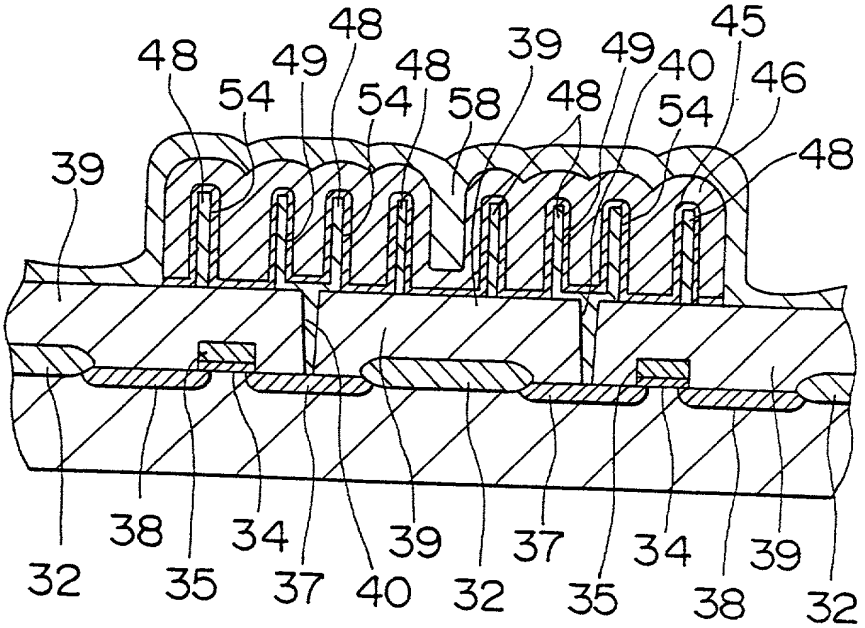

Fig.12E

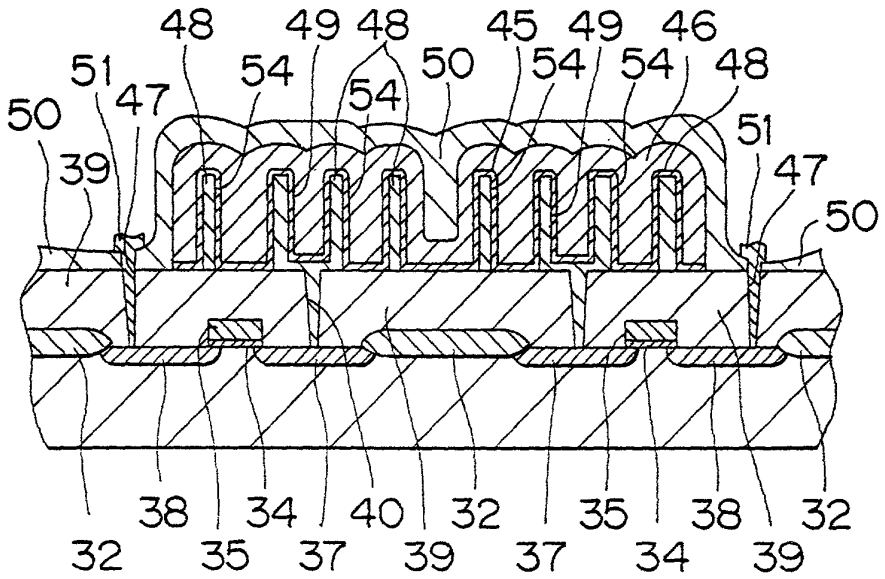
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Fig.13

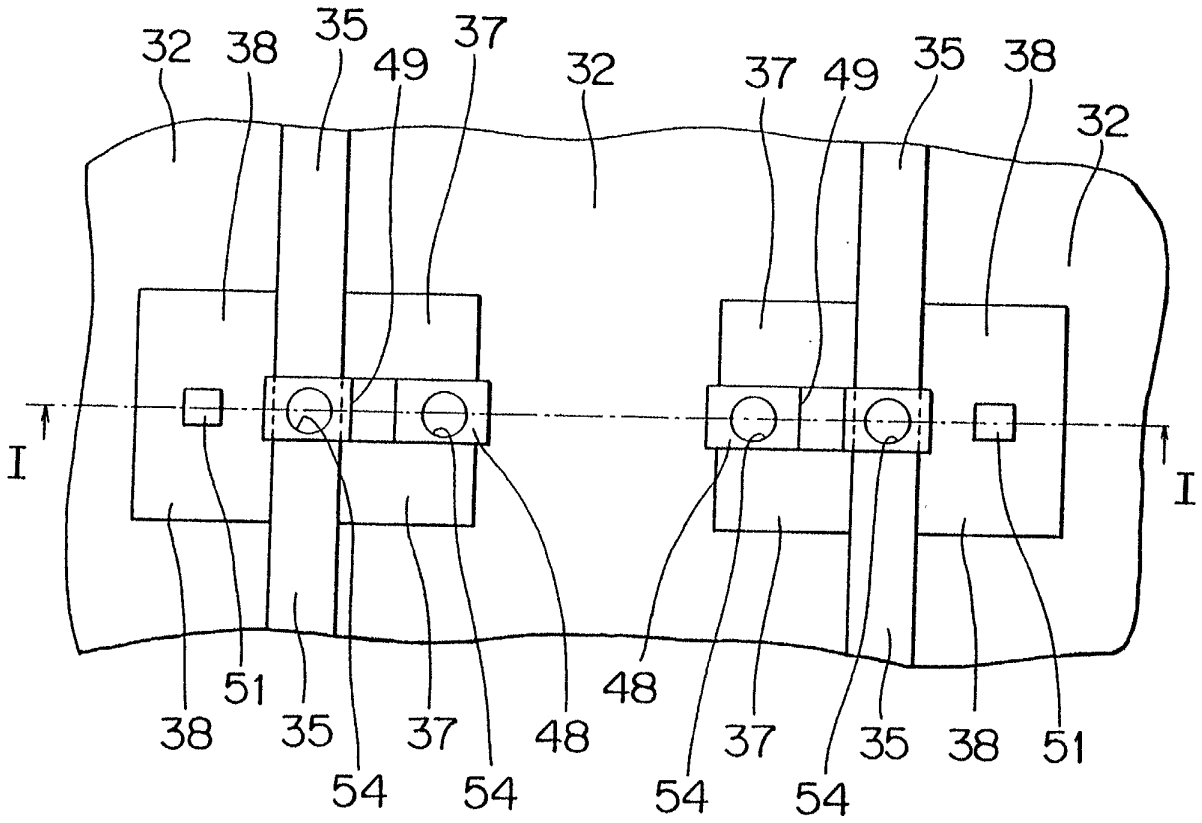


Fig.14A

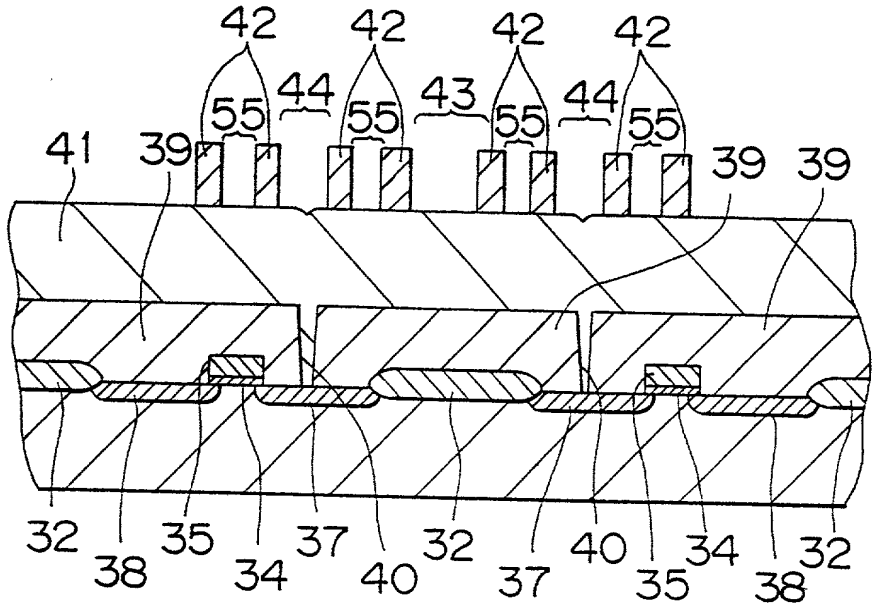


Fig.14B

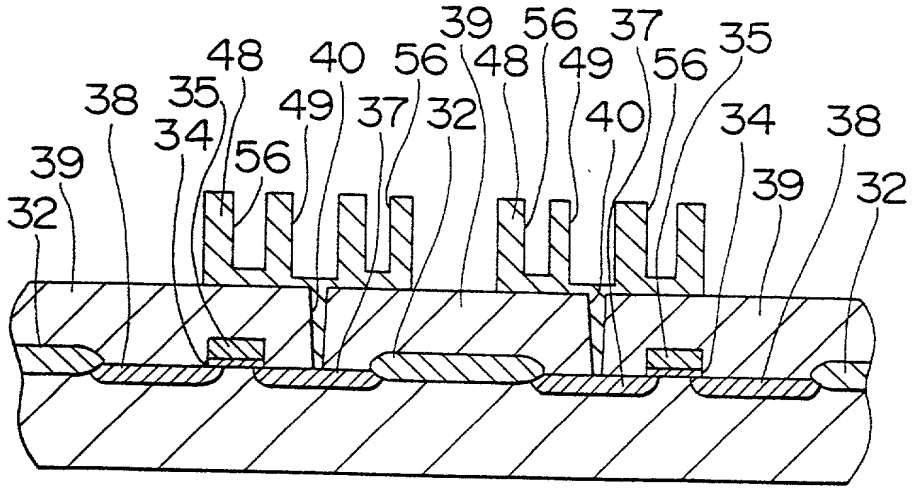


Fig.14C

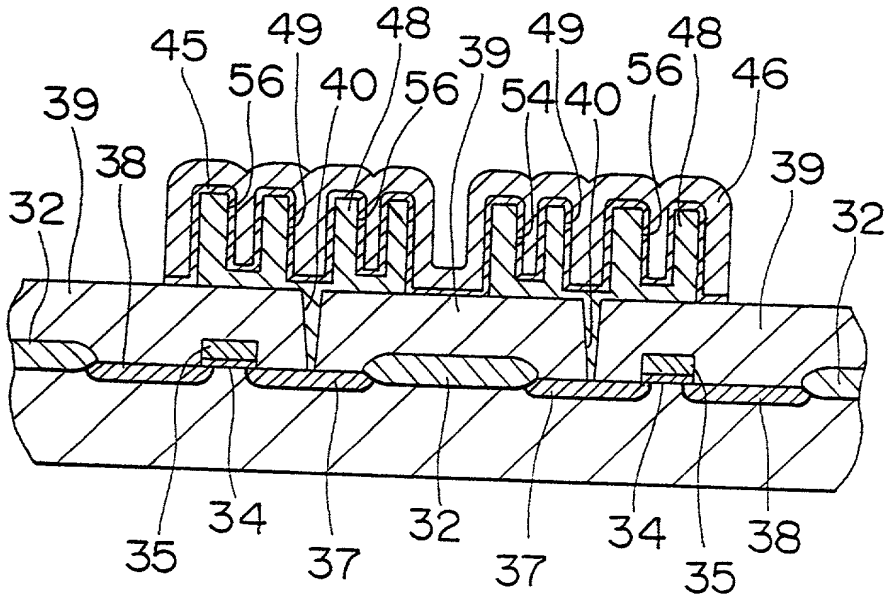


Fig.14D

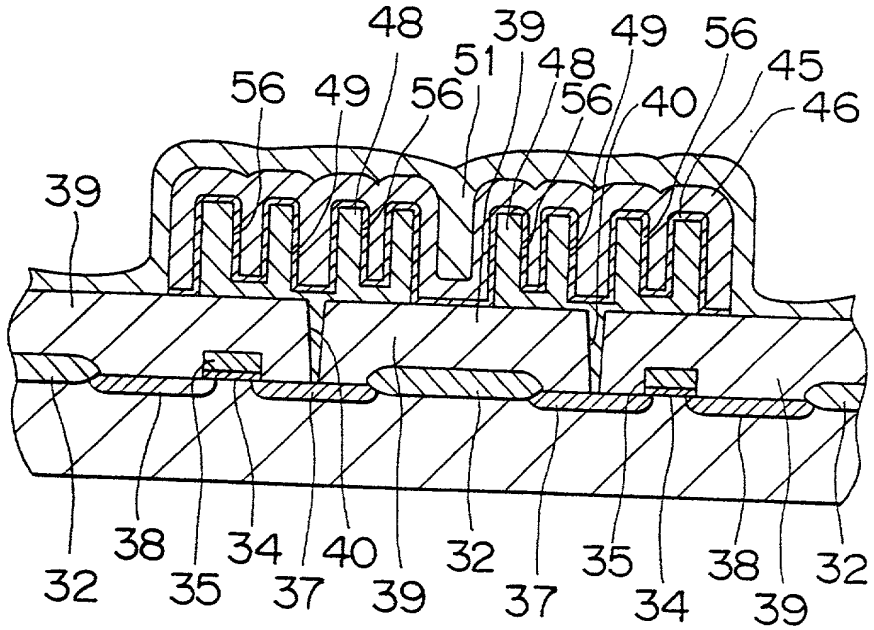
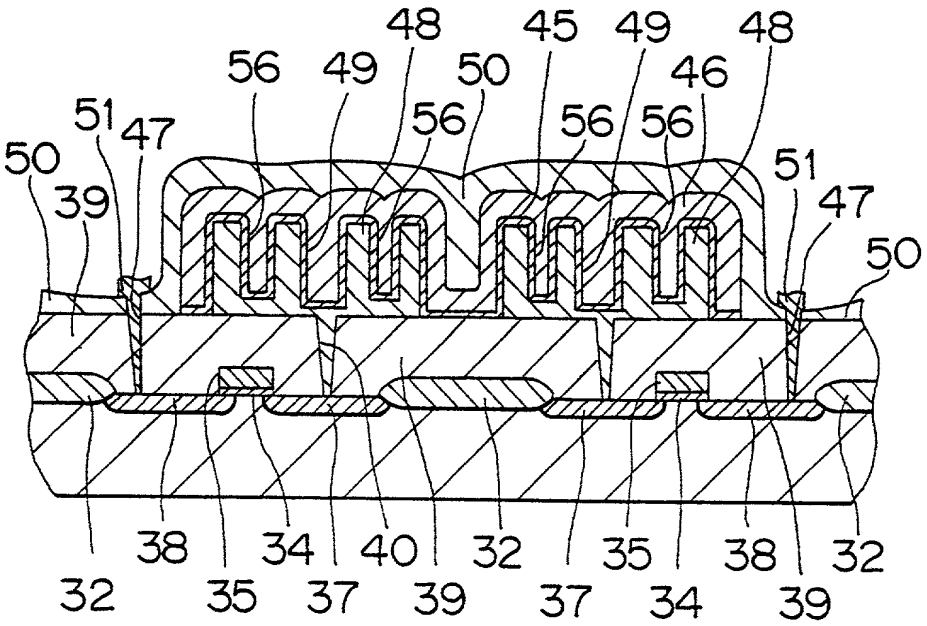


Fig.14E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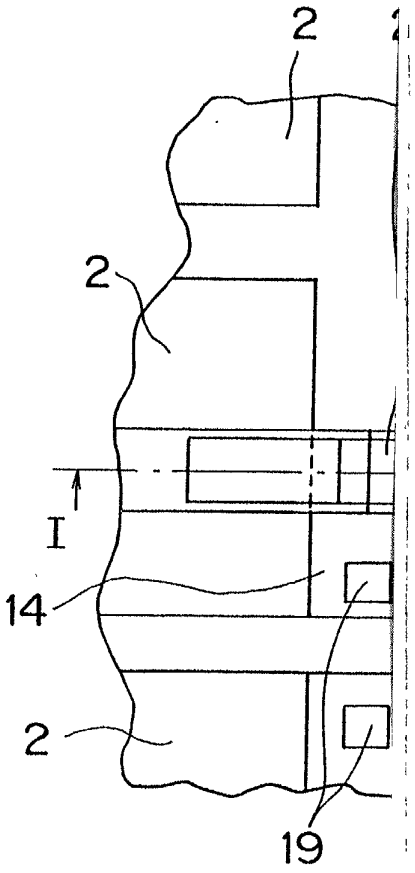


Fig.15

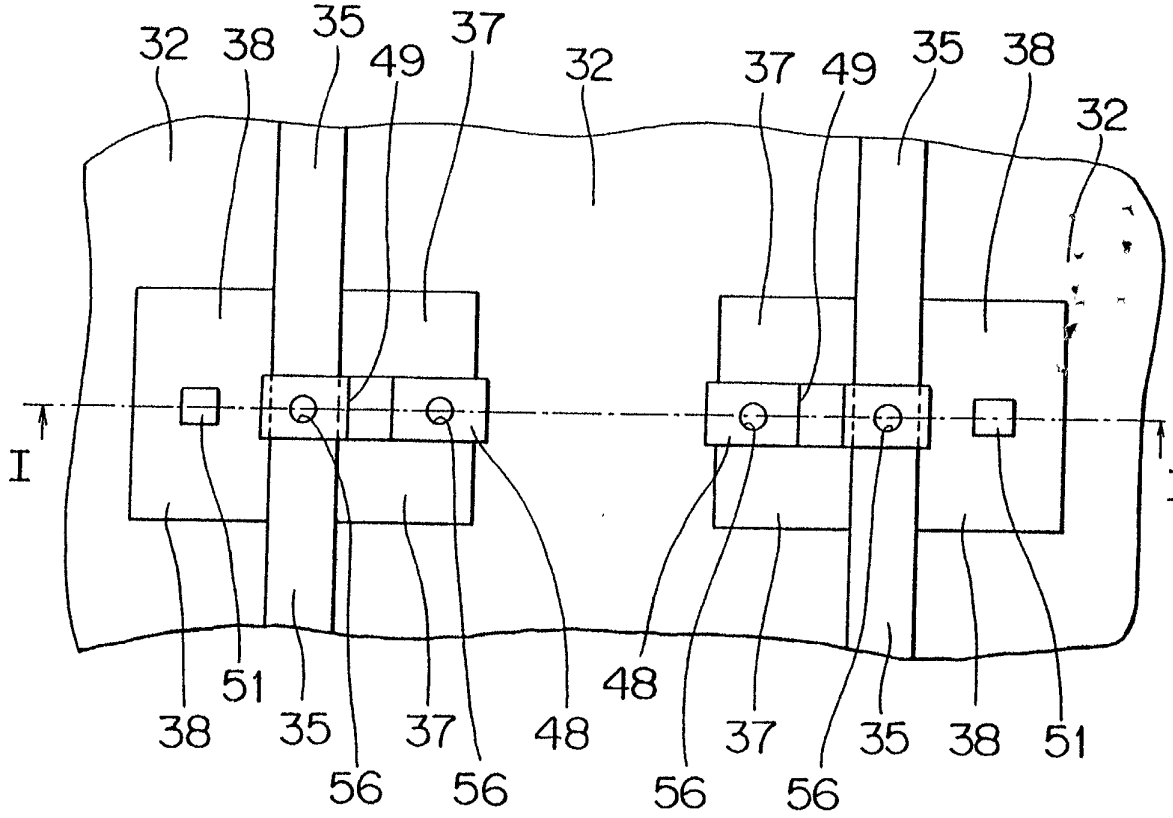


Fig. 16

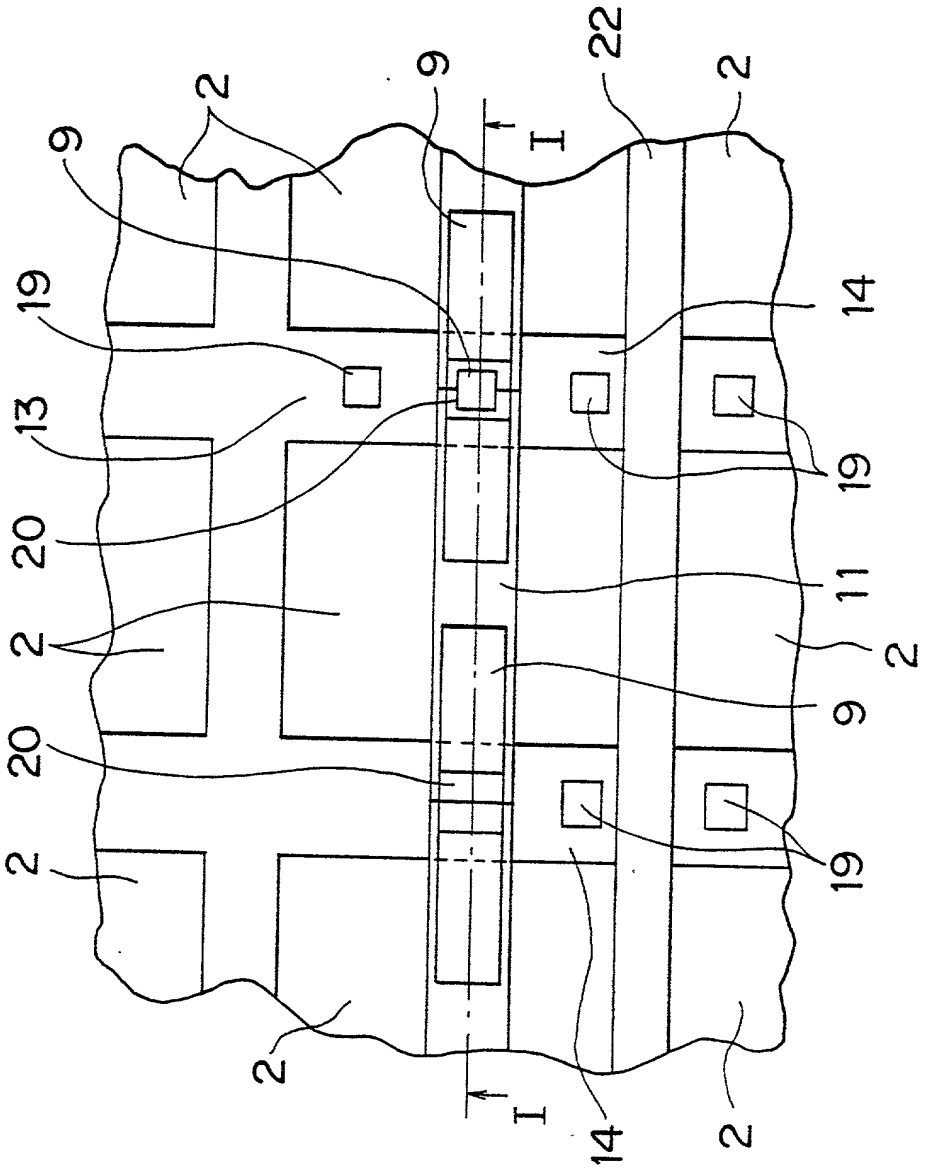
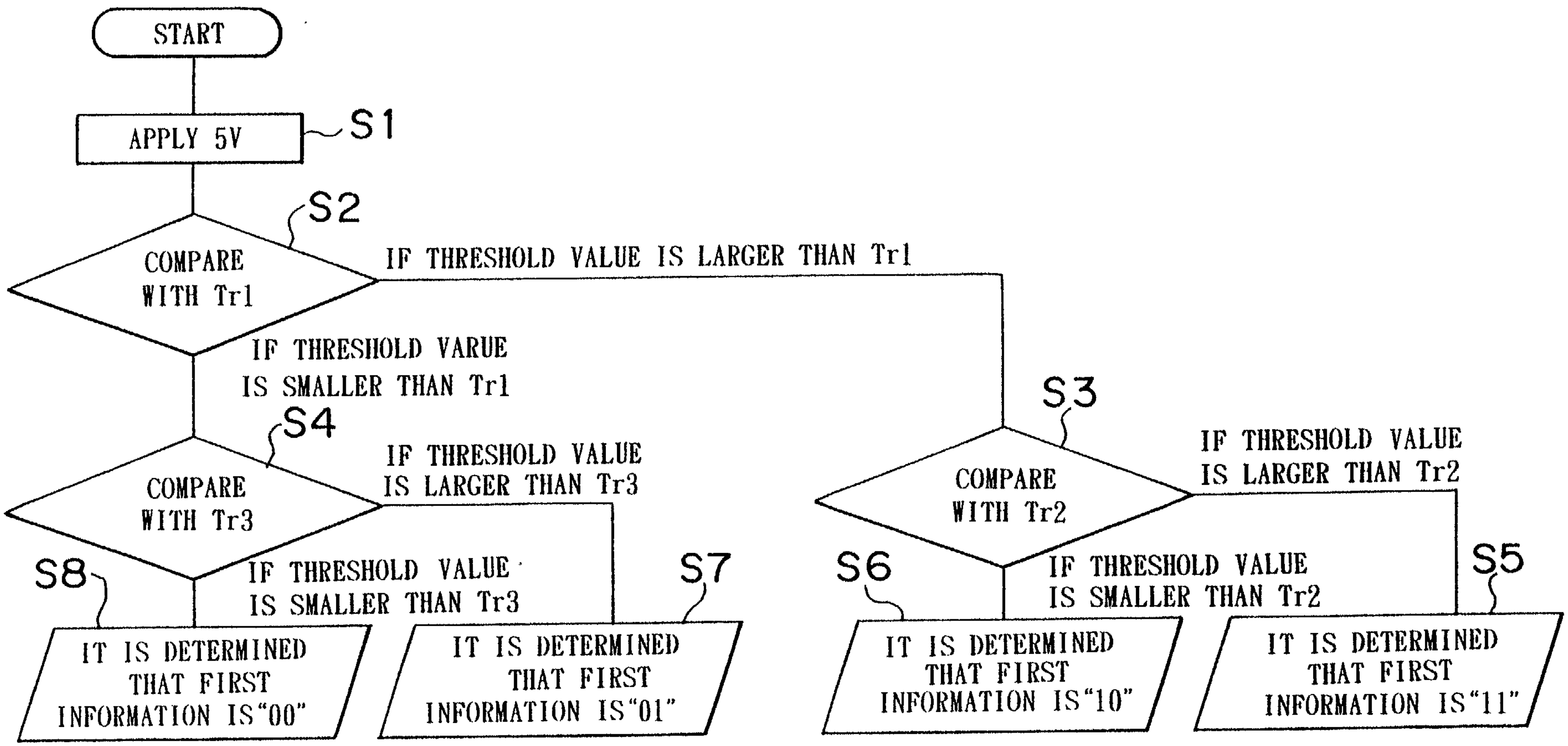


Fig.17


START
APPLY 5V
S1
S2
COMPARE WITH Tr1
IF THRESHOLD VALUE IS LARGER THAN Tr1
IF THRESHOLD VARUE IS SMALLER THAN Tr1
S4
COMPARE WITH Tr3
IF THRESHOLD VALUE IS LARGER THAN Tr3
IF THRESHOLD VALUE IS SMALLER THAN Tr3
S8
IT IS DETERMINED THAT FIRST INFORMATION IS"00"
S7
IT IS DETERMINED THAT FIRST INFORMATION IS"01"
S3
COMPARE WITH Tr2
IF THRESHOLD VALUE IS LARGER THAN Tr2
IF THRESHOLD VALUE IS SMALLER THAN Tr2
S6
IT IS DETERMINED THAT FIRST INFORMATION IS"10"
S5
IT IS DETERMINED THAT FIRST INFORMATION IS"11"

DECLARATION AND POWER OF ATTORNEY

U.S.A.

As a below-named inventor, I hereby declare: My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled A SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME, the specification of which

☒ is attached hereto.

☐ was filed on _____, as application Serial No. _____, and was amended on _____(if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above, and acknowledge a duty to disclose information which is material to the examination of this application under 37 CFR 1.56(a). I hereby claim priority benefits under 35 U.S.C. §119 based on any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate on the present invention, filed before the application(s) in which priority is claimed.

FOREIGN APPLICATION(S), IF ANY, REFERRED TO ABOVE			
COUNTRY	APPLICATION NO.	DATE	PRIORITY CLAIMED
JAPAN	9-116322	April 18, 1997	YES X NO ___
			YES ___ NO ___
			YES ___ NO ___

I hereby claim benefit under 35 U.S.C. §120 of any U.S. application(s) listed below. If the subject matter of any claim(s) of this application is not disclosed in the prior U.S. application(s) as required by paragraph one of 35 U.S.C. §112, I acknowledge a duty to disclose material information as defined in 37 CFR 1.56(a) regarding occurrences between the filing date of the prior application(s) and the national or PCT international filing date of this application.

SERIAL NUMBER	FILING DATE	STATUS

I hereby appoint Elliott I. Pollock, RN (Registration No.) 16,906; George Vande Sande, RN 17,276; Robert R. Priddy, RN 20,169; Burton A. Amernick, RN 24,852; Stanley B. Green, RN 24,351; Richard Wiener, RN 18,741; Townsend M. Belser, Jr., RN 22,956; Morris Liss, RN 24,510; Martin Abramson, RN 25,787; George R. Pettit, RN 27,369; Louis Woo, RN 31,730; Elzbieta Chlopecka, RN 32,767; and Eric Franklin, RN 37,134, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Address all communications to Pollock, Vande Sande & Priddy, P.O. Box 19088, Washington, D. C. 20036-3425.

All statements made herein of my own knowledge are true. All statements made on information and belief are believed to be true. These statements were made with the knowledge that willful false statements and the like so made are punishable by fine, imprisonment, or both, under 18 U.S.C. 1001 and may jeopardize the validity of the application or any patent issuing thereon.

Note: Please sign one full given name and your surname, using initials where appropriate for other names. It is important that the name be consistent throughout the application papers. Signing of an application more than five weeks prior to filing or an undated application is not acceptable to the Patent and Trademark Office except for receiving an initial filing date.

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2. Full name of inventor _____ Date: _____

Inventor's signature _____

Residence _____

Citizenship _____

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☐ See additional page for additional inventors, if checked.